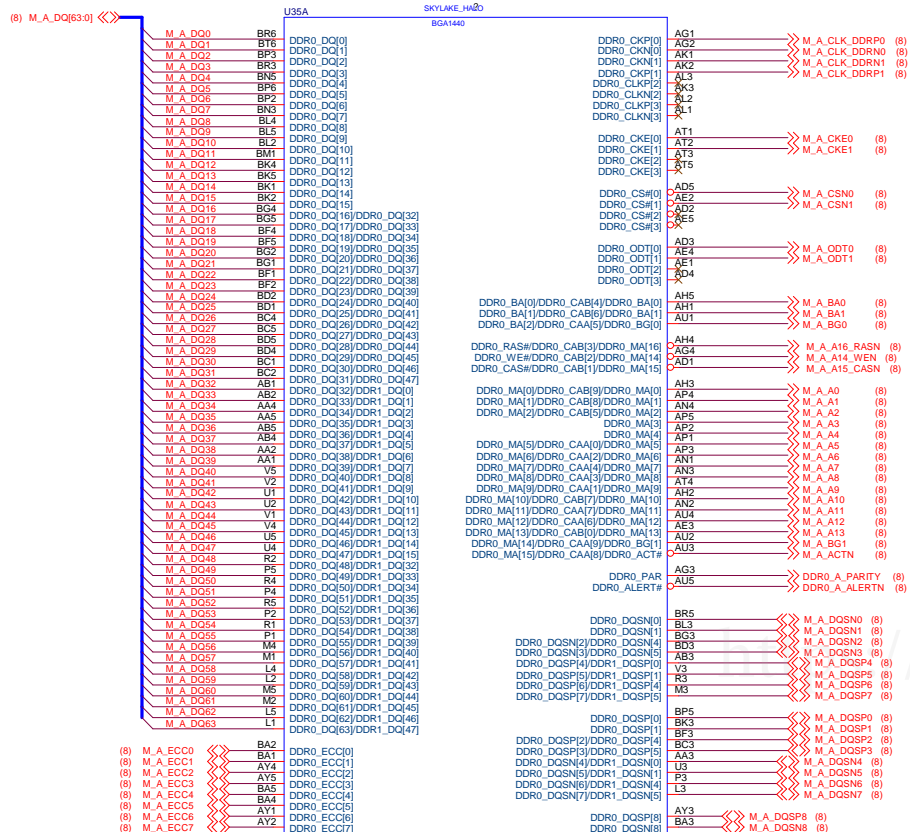
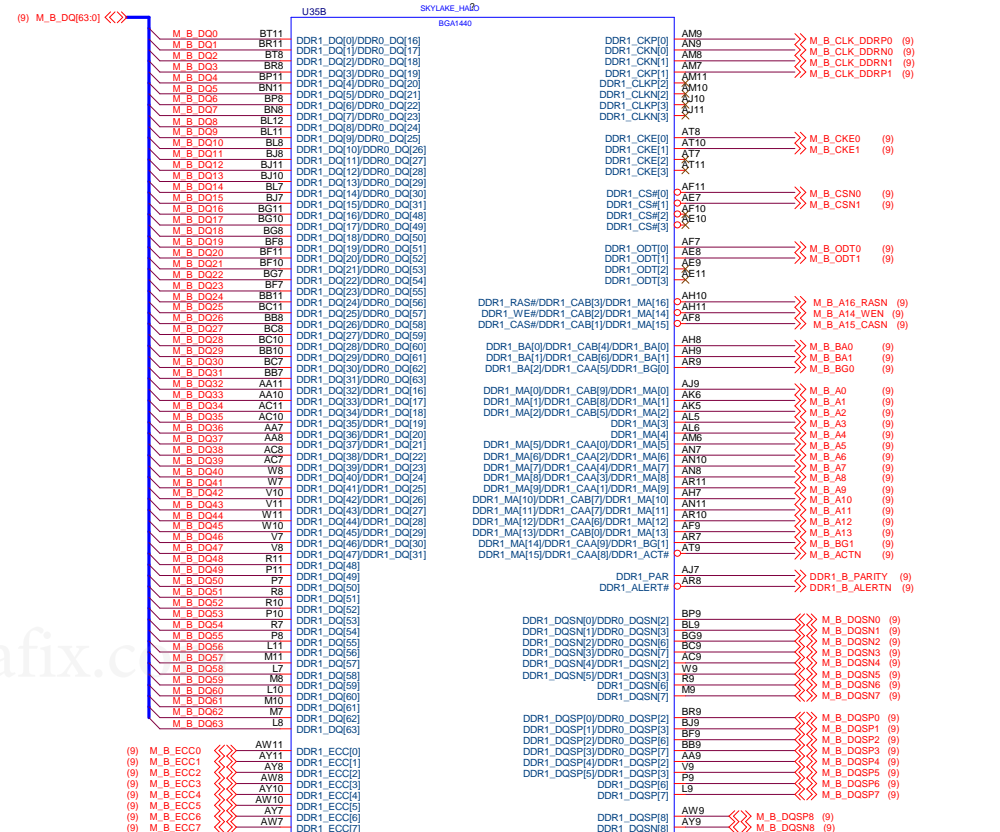
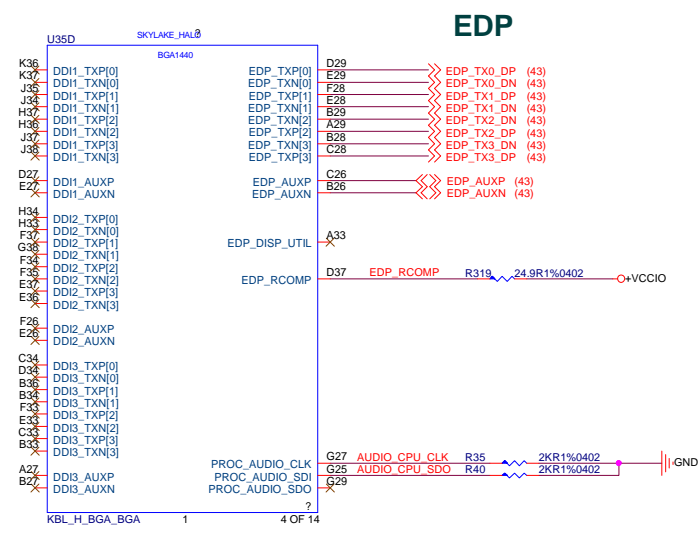
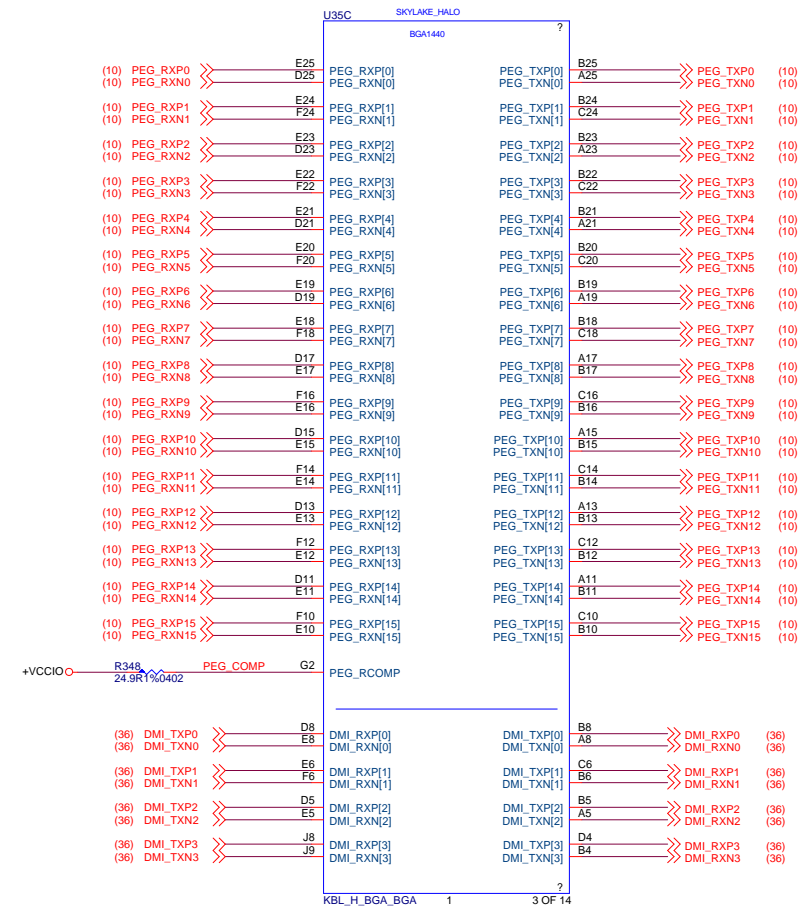


DDR Channel A



DDR Channel B

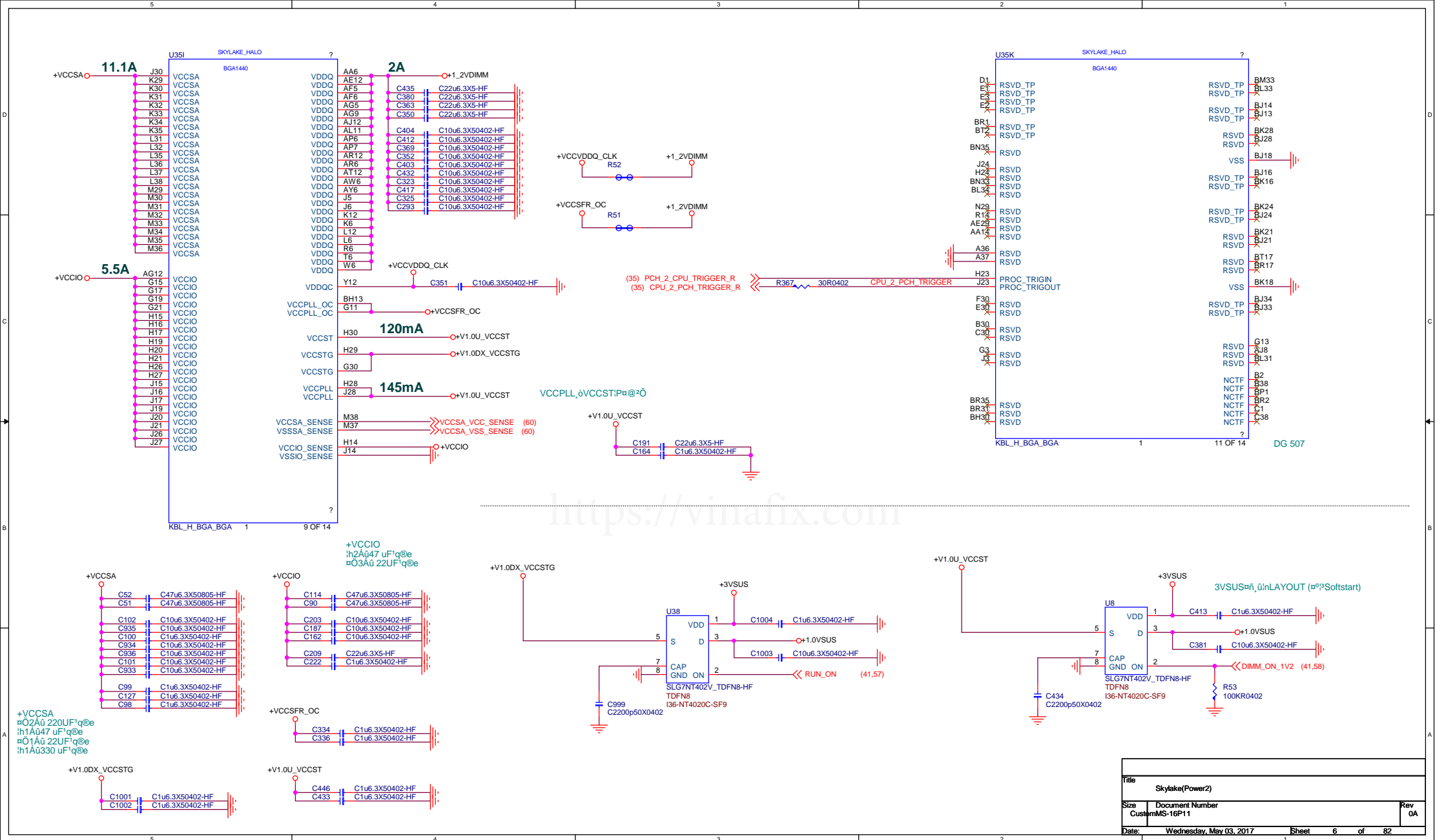


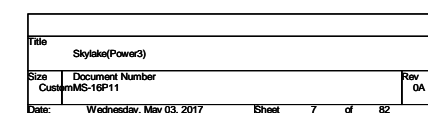


EDP

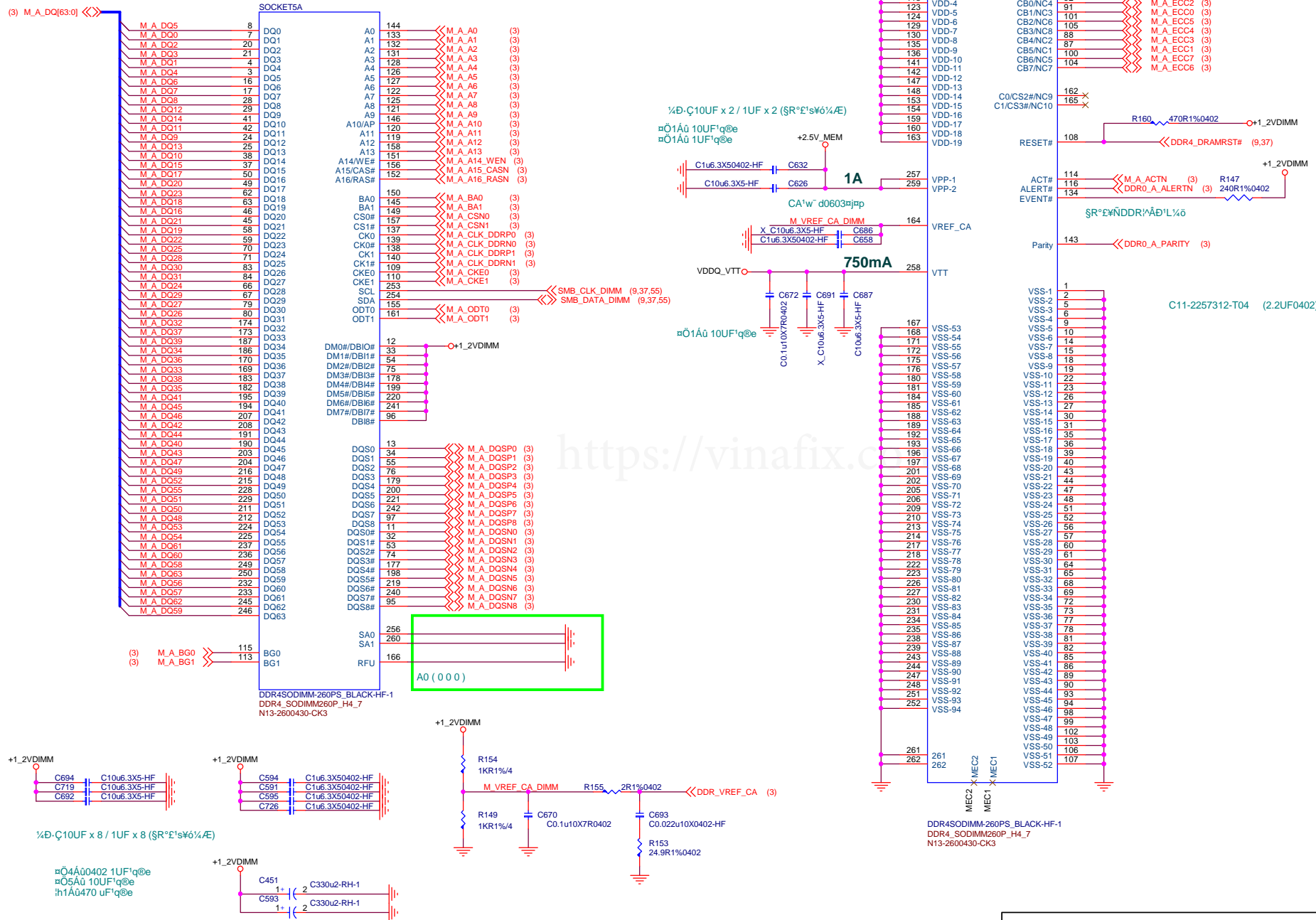
<https://vinafix.com>

Title				
Skylake(DMI/Display)				
Size	Document Number			Rev
Custom	MS-16P11			0A
Date:	Wednesday, May 03, 2017	Sheet	4	of 82



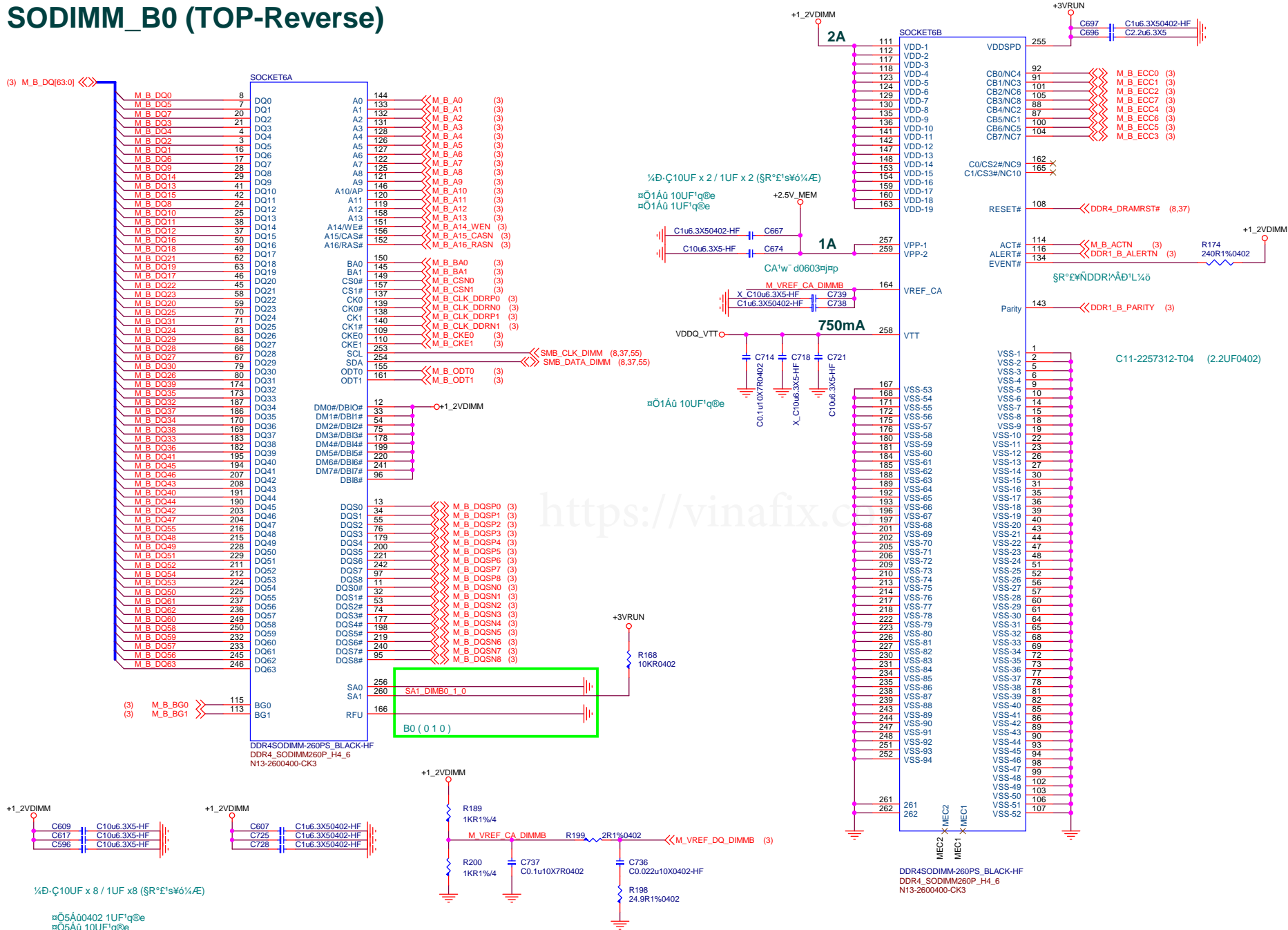


SODIMM_A0 (TOP-Standard)



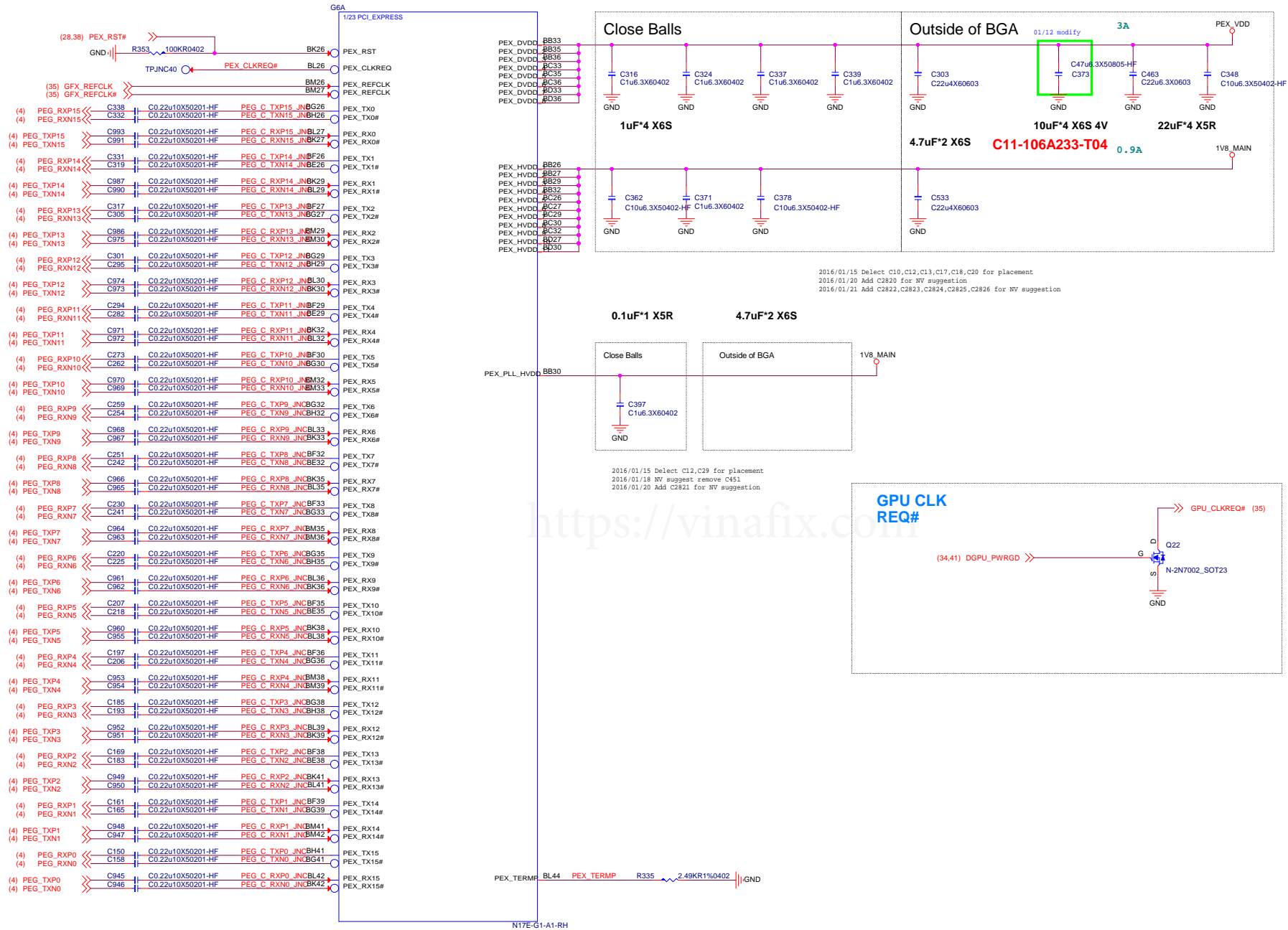
Title		
DDR4_SODIMM_A0		
Size	Document Number	Rev
CustomMS-16P11		0A
Date:	Wednesday, May 03, 2017	Sheet 8 of 82

SODIMM_B0 (TOP-Reverse)

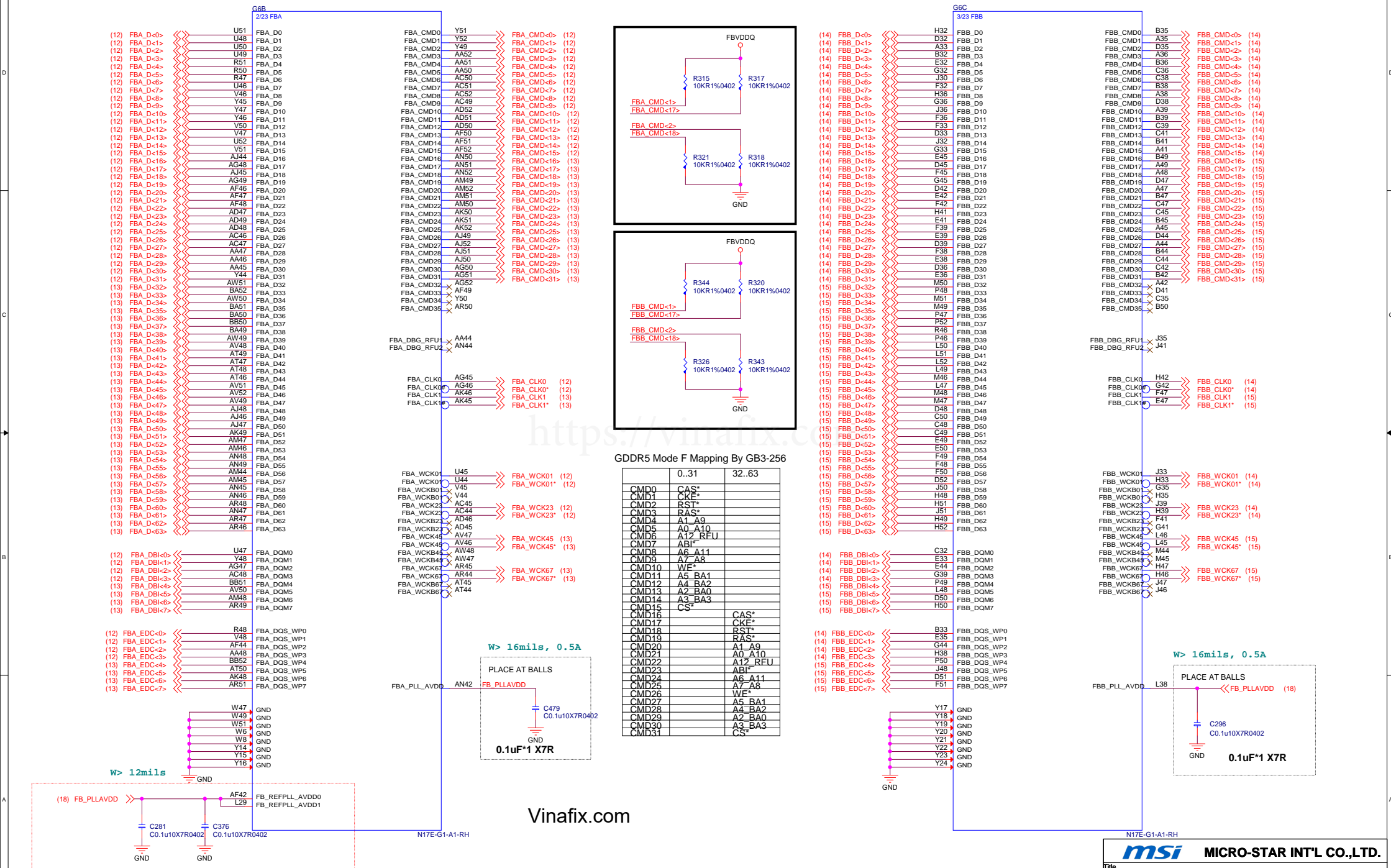


Title			
DDR4_SODIMM_B0			
Size	Document Number	Rev	
Custom	MS-16P11	0/	
Date:	Wednesday, May 03, 2017	Sheet	9 of 82

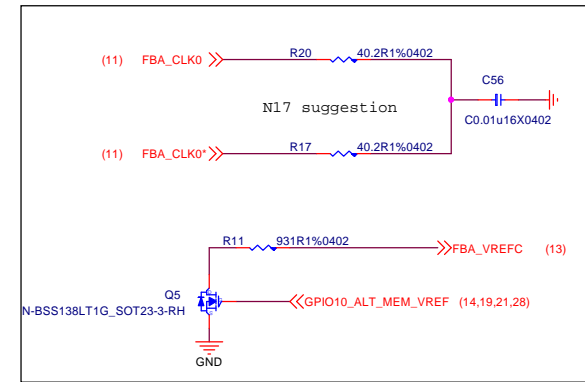
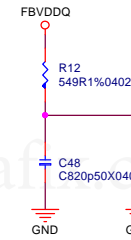
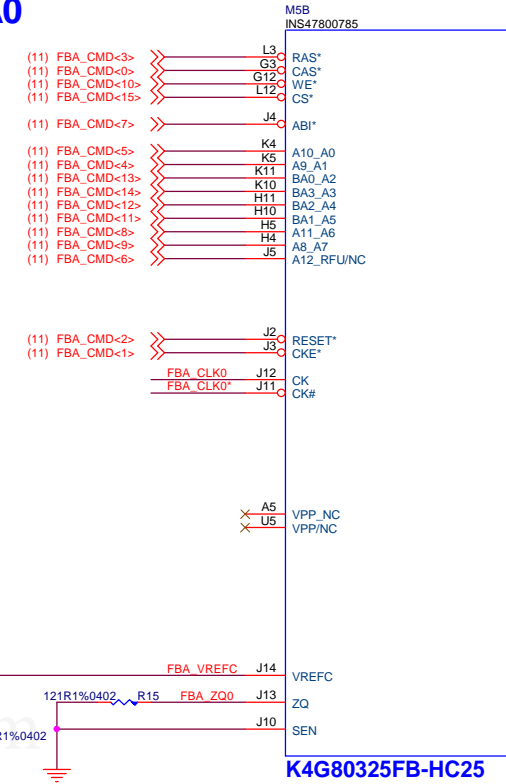
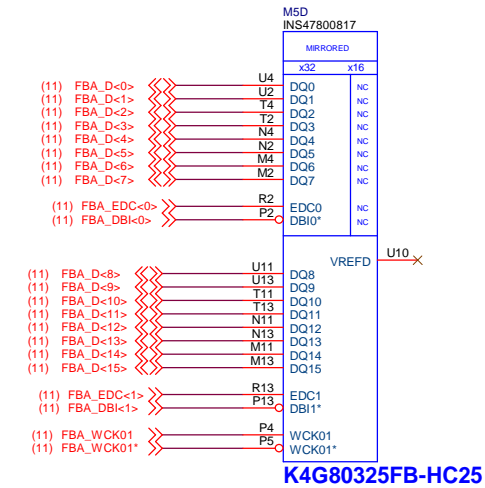
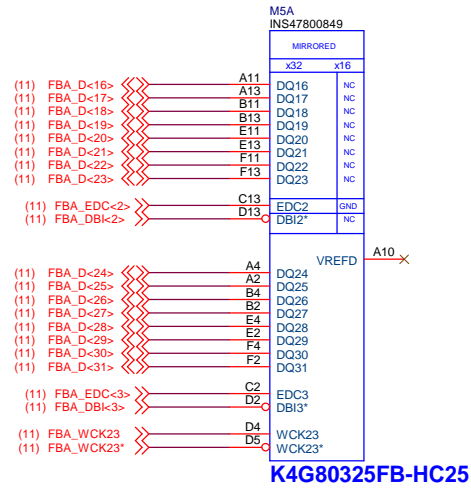
GPU PCI EXPRESS



GPU Frame Buffer Partition A/B



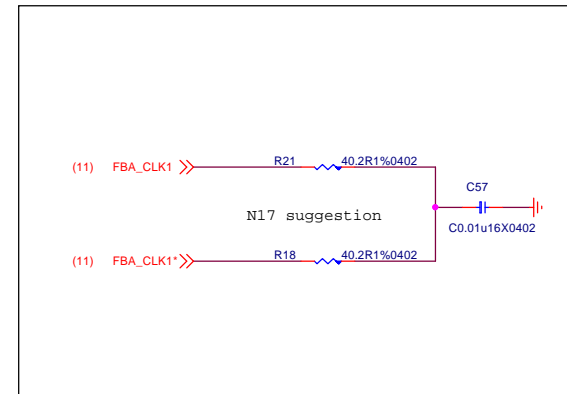
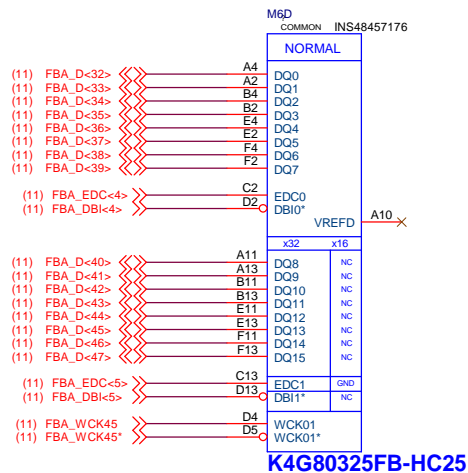
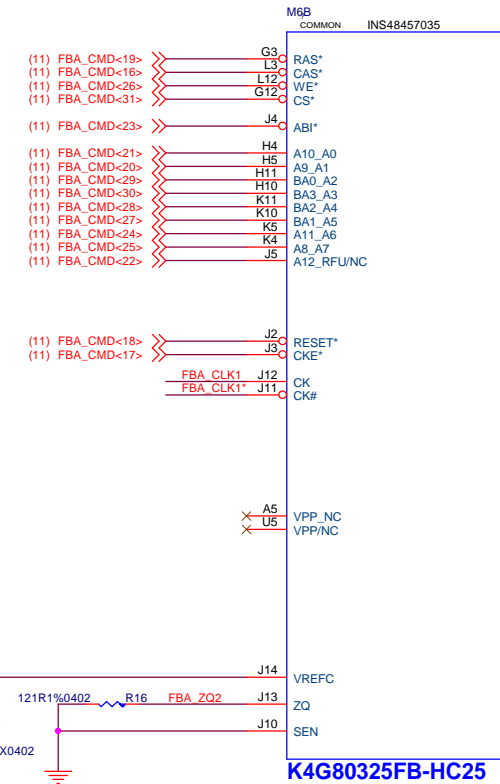
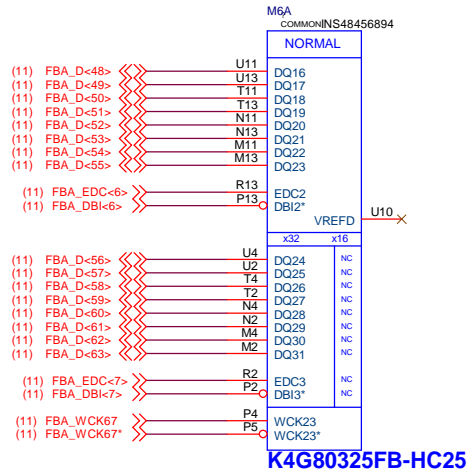
DGPU_GDDR5 FrameBuffer A0



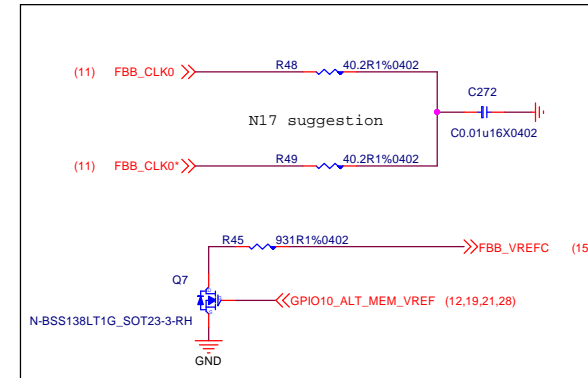
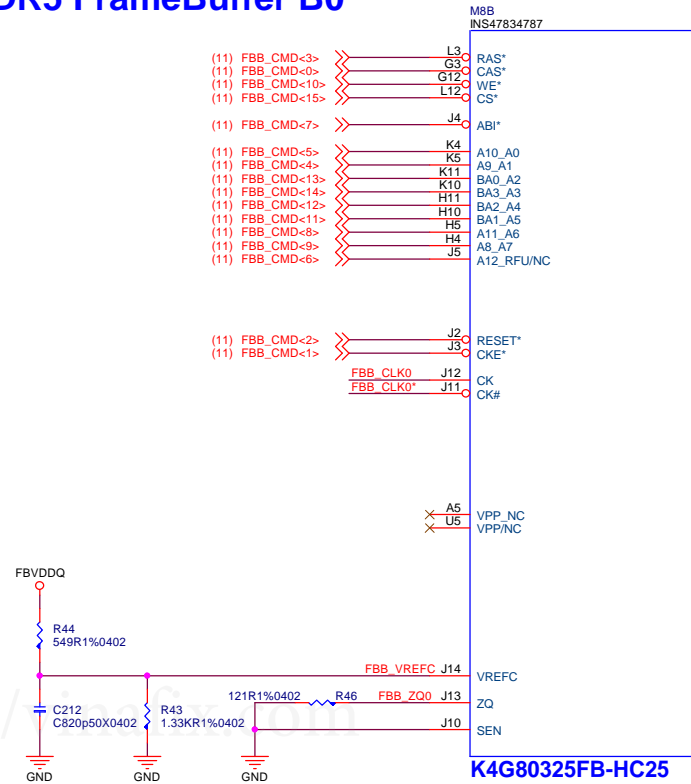
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Hynix PN : M12-5GC4H65-H23 3G(128Mx32bit)
Samsung PN : M12-4132525-S02 3G(128Mx32bit)

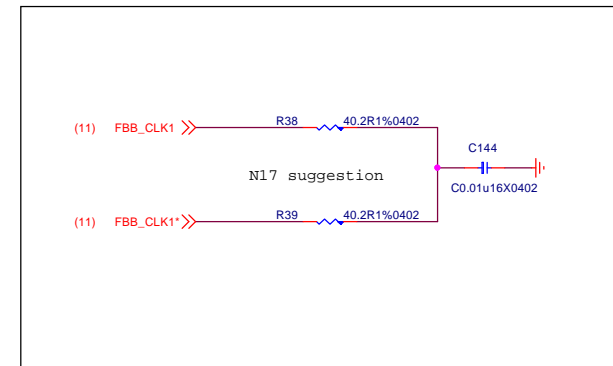
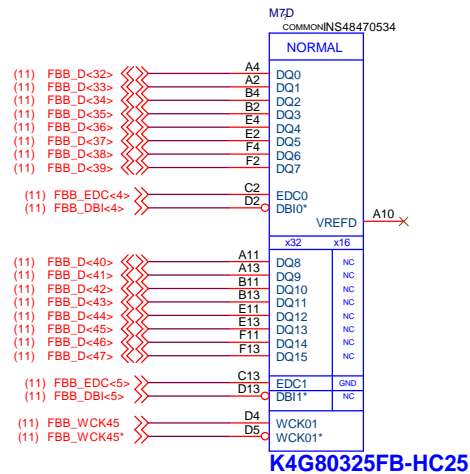
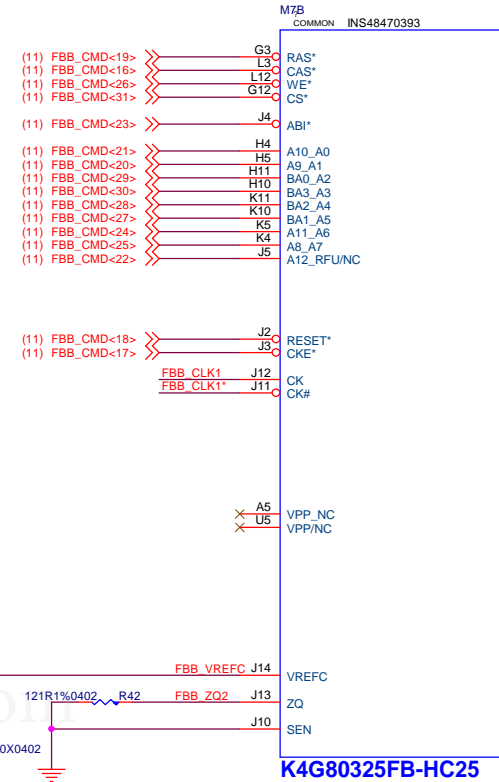
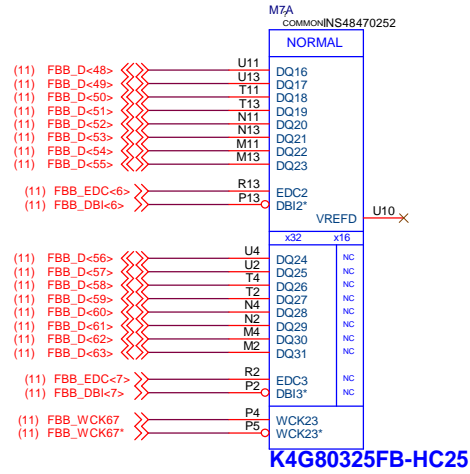
DGPU_GDDR5 FrameBuffer A1



121R1%0402 R46

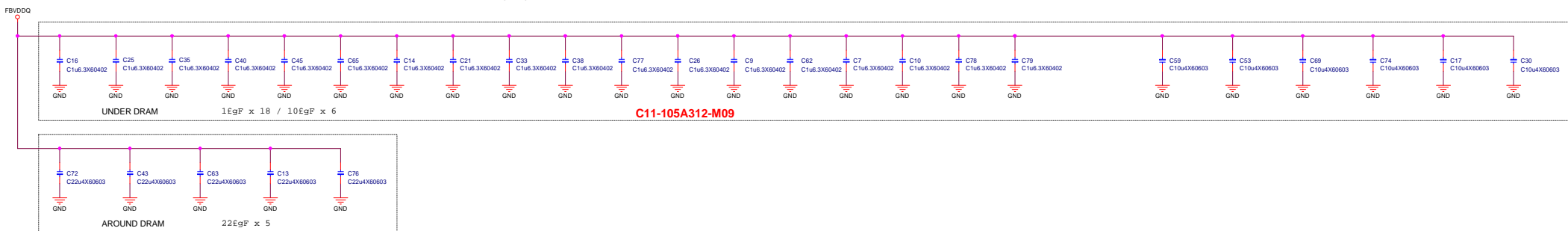
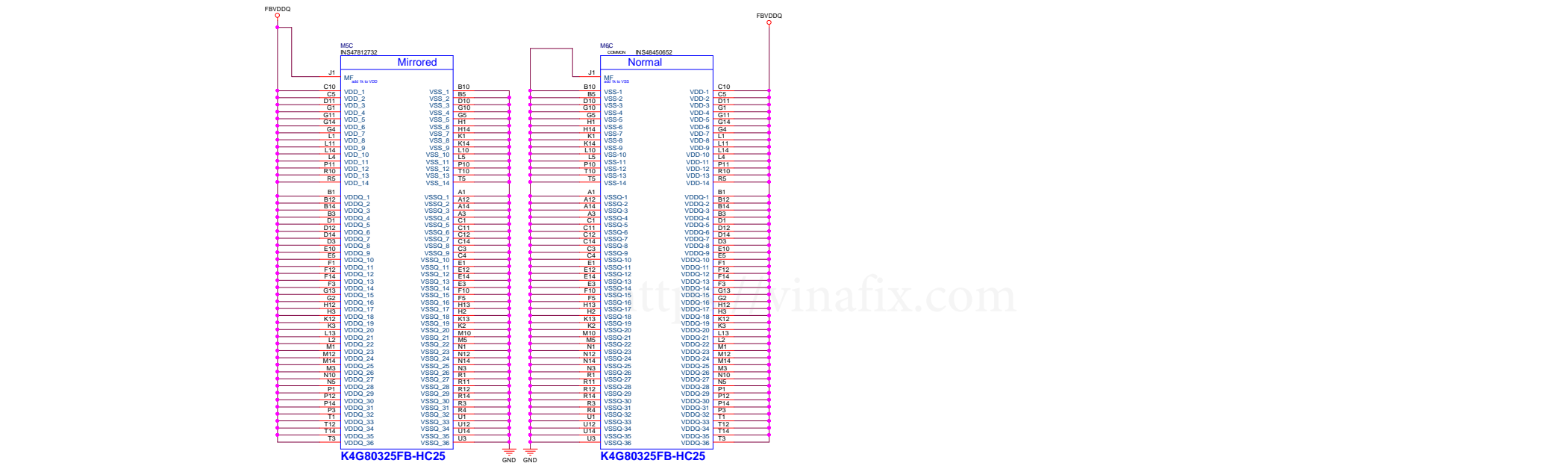
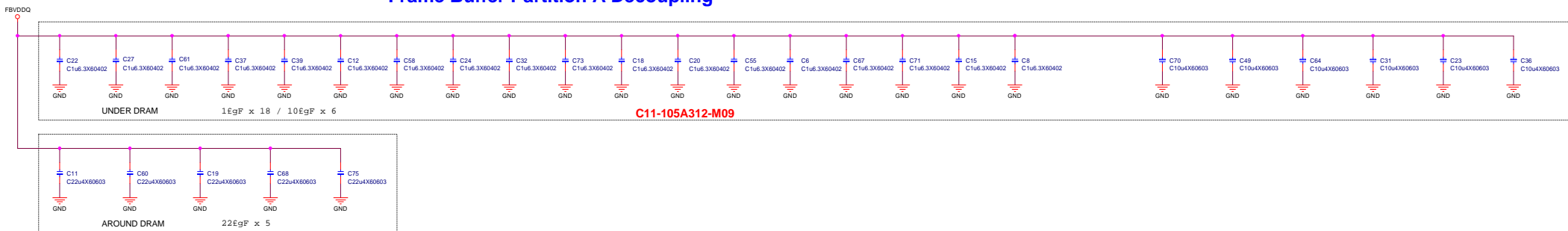


DGPU_GDDR5 FrameBuffer B1

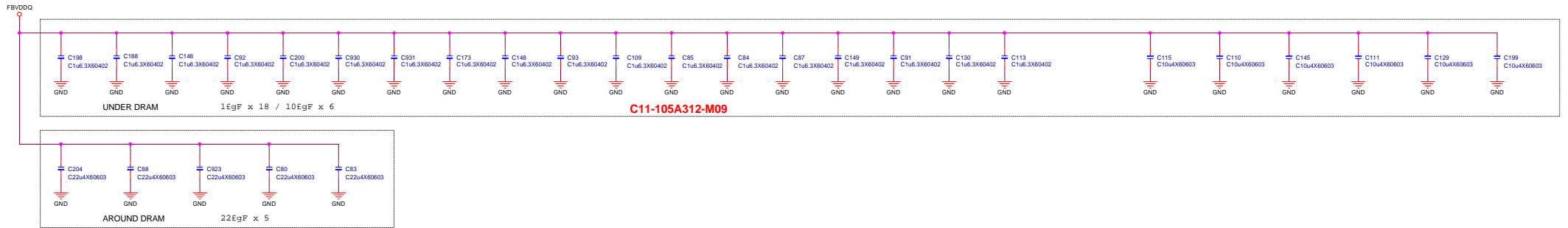
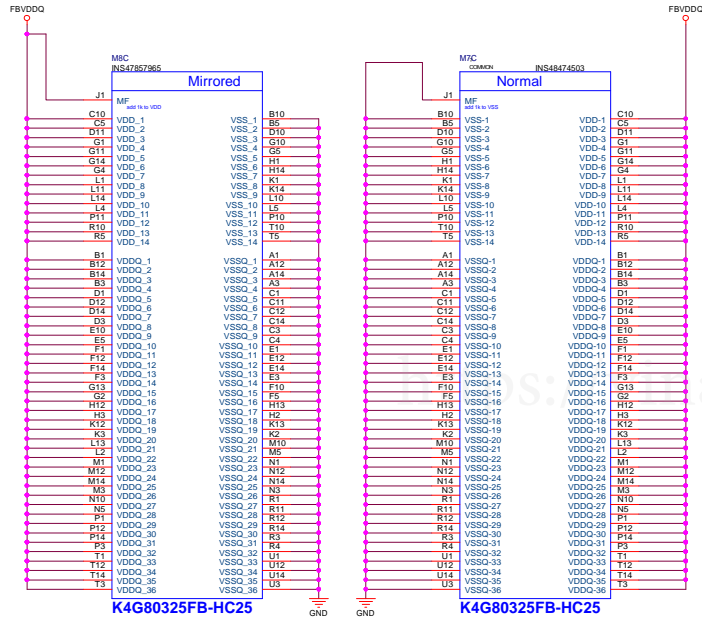
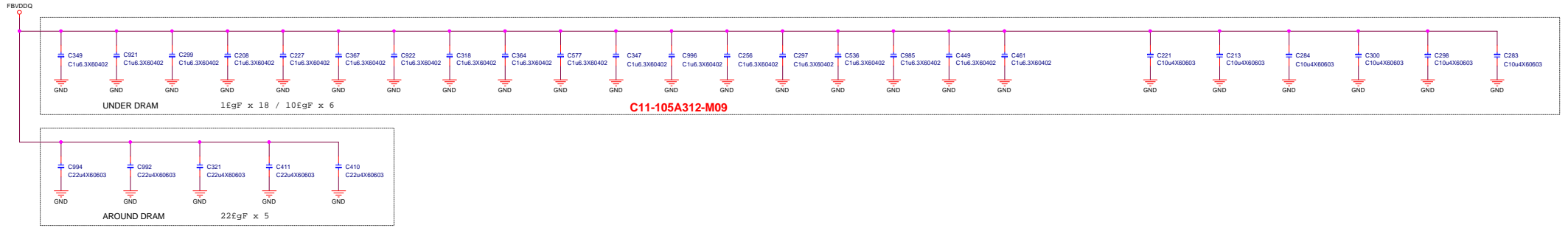


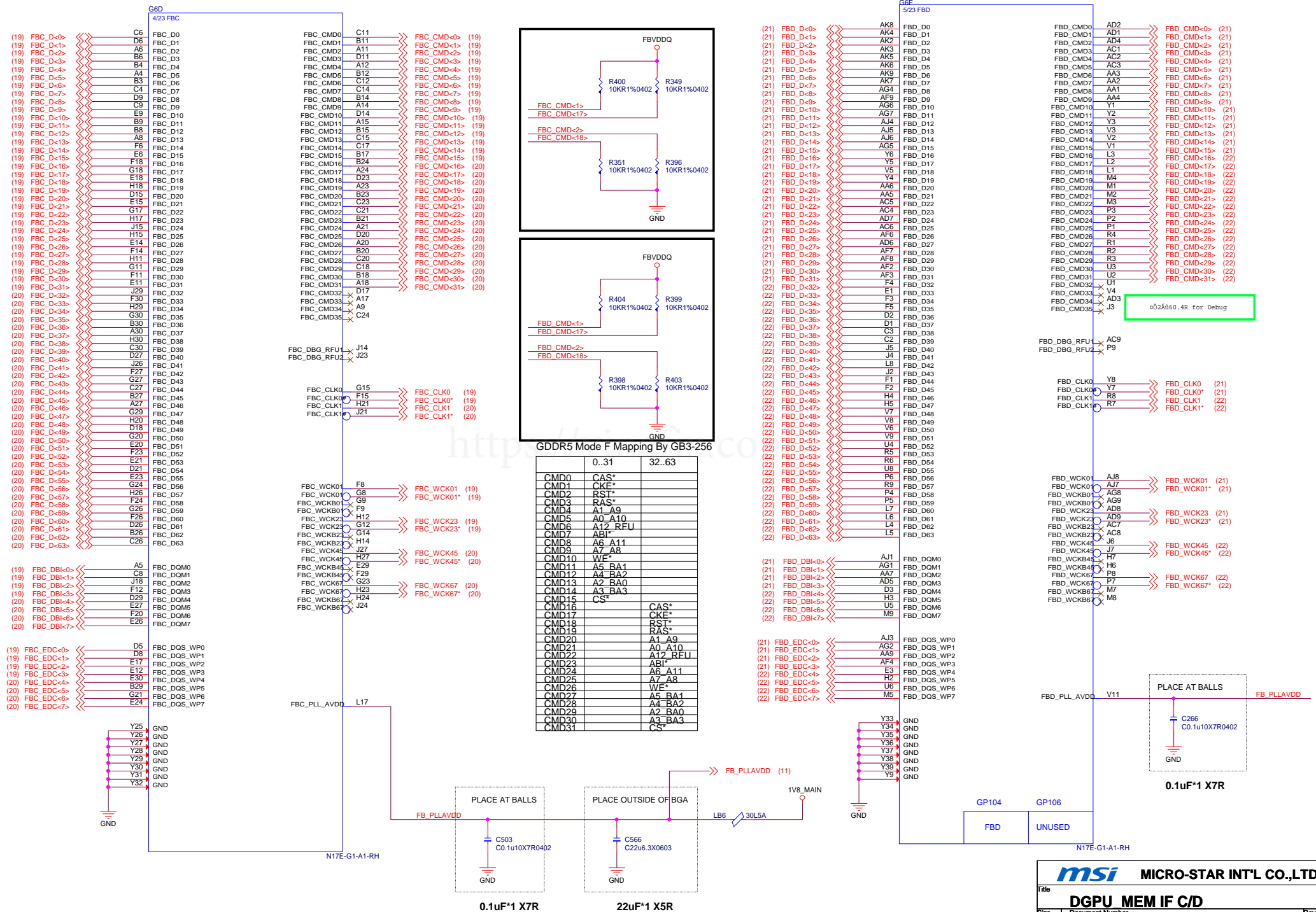
Vinafix.com

Frame Buffer Partition A Decoupling

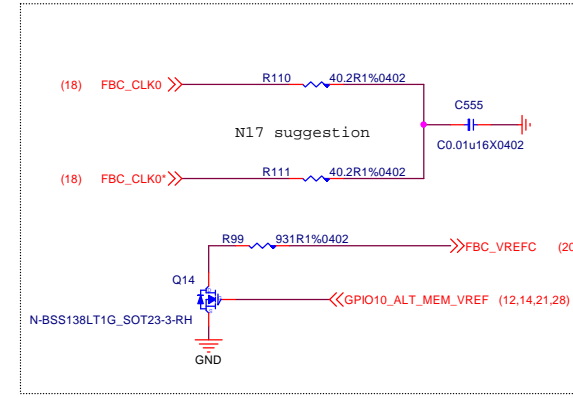
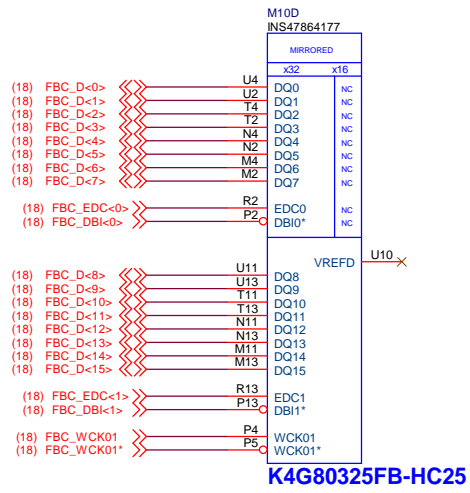
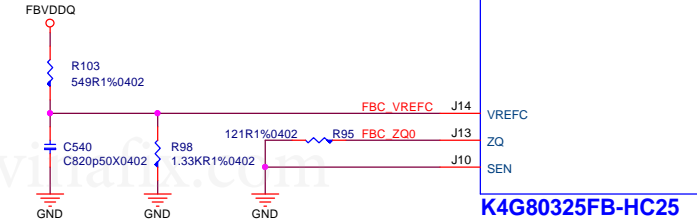
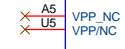
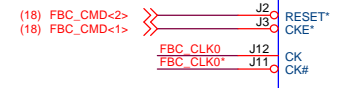
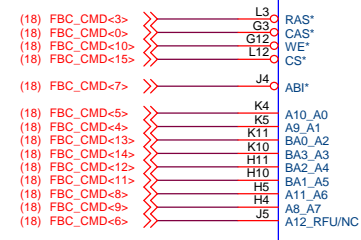
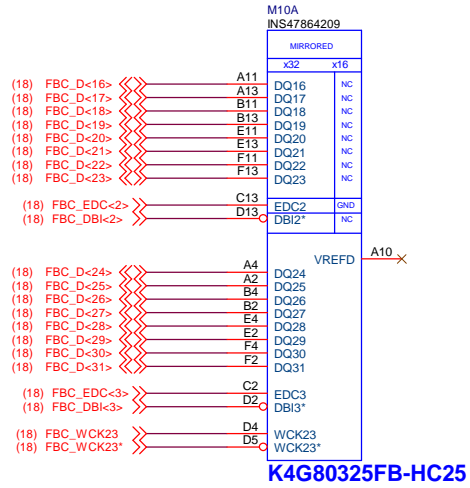


Frame Buffer Partition B Decoupling

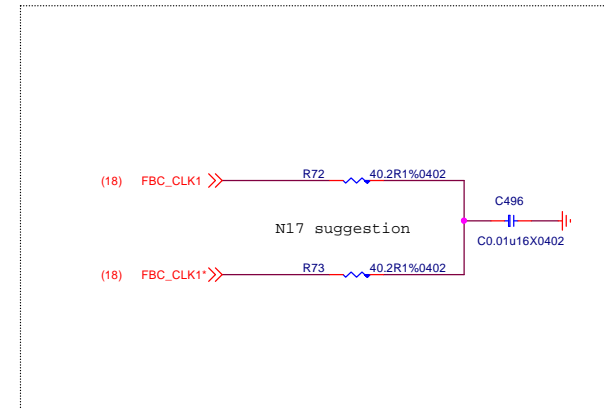
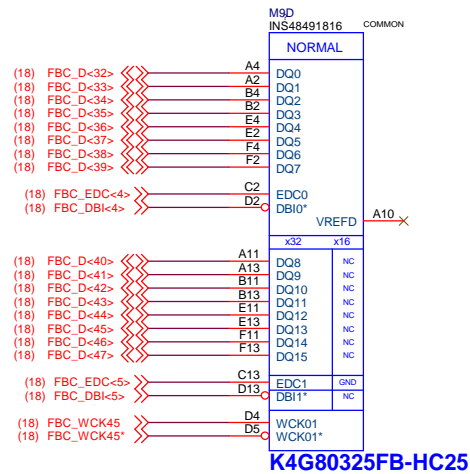
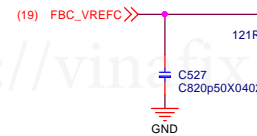
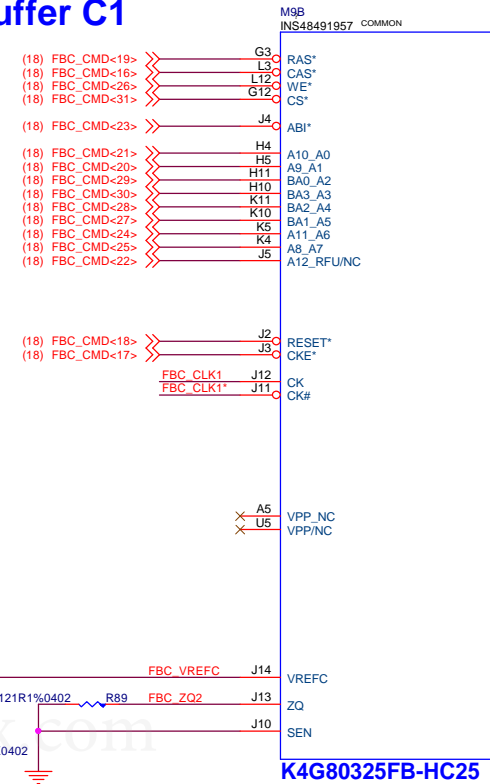
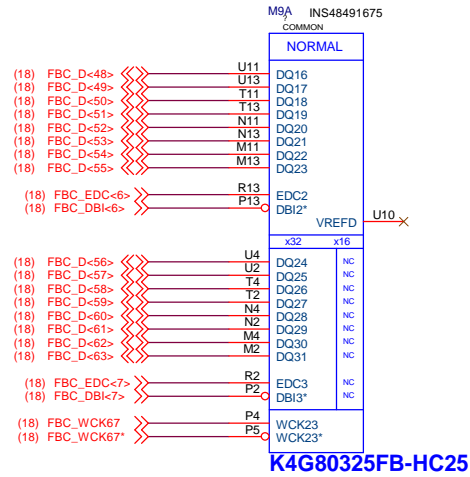




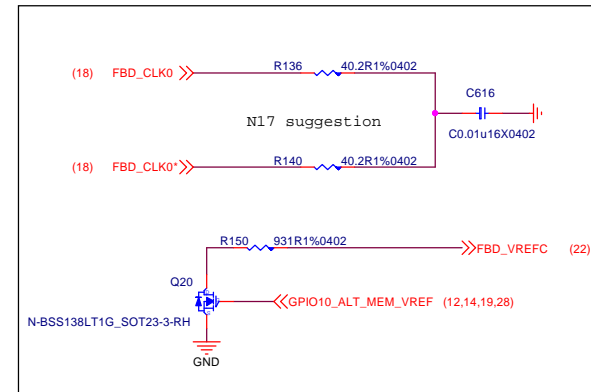
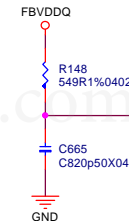
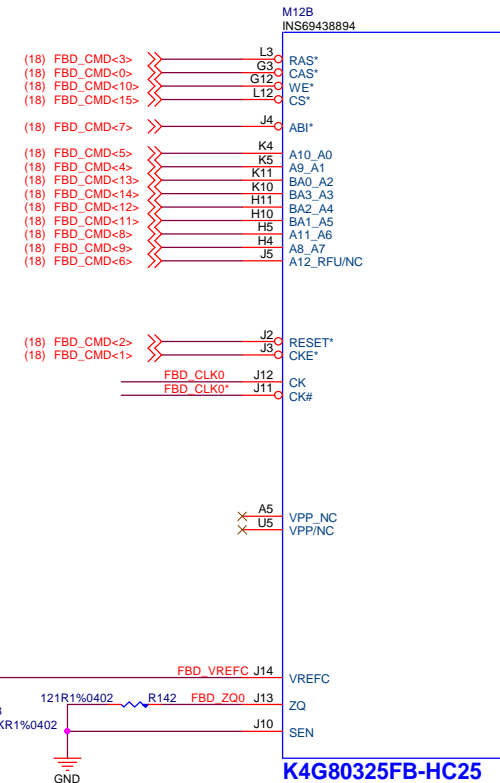
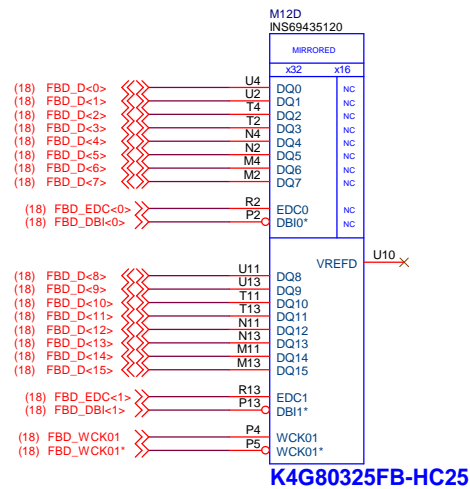
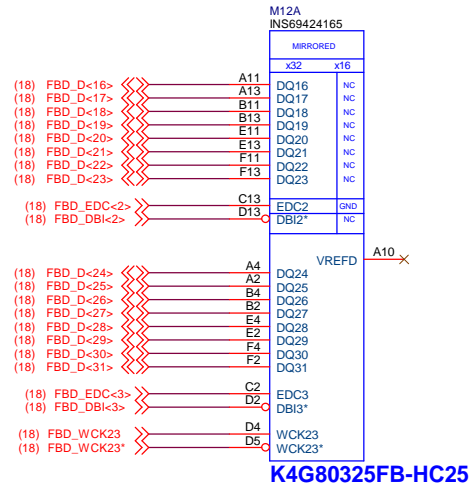
DGPU_GDDR5 FrameBuffer C0



DGPU_GDDR5 FrameBuffer C1

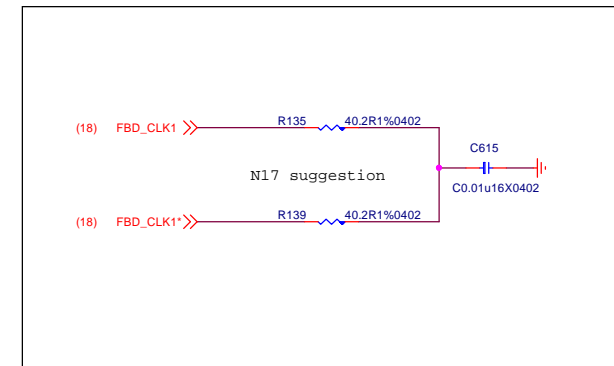
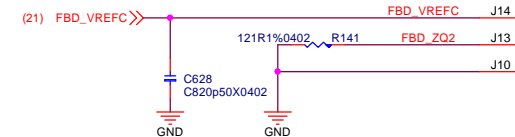
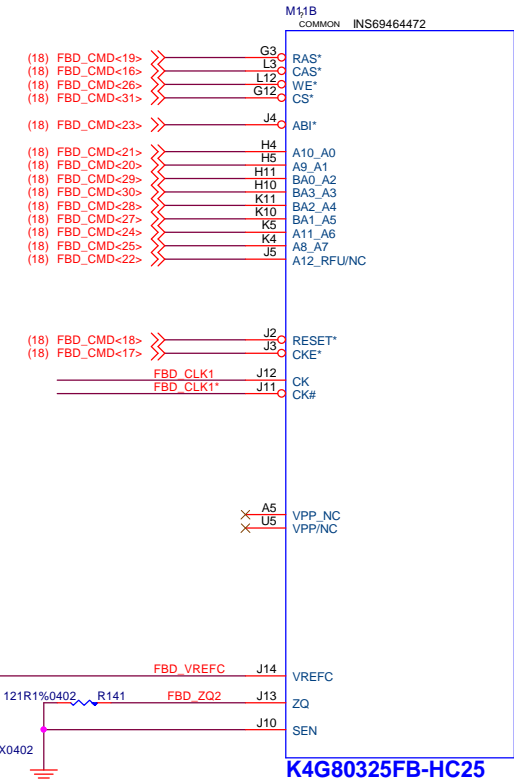
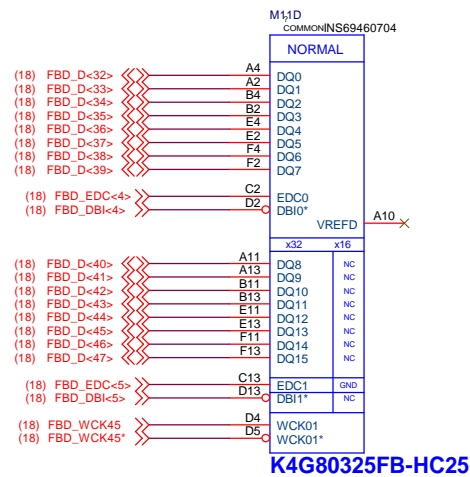
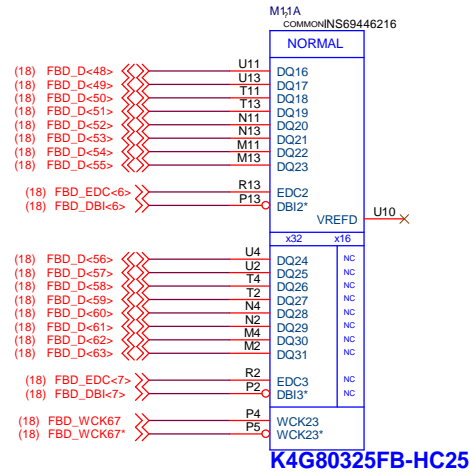


DGPU_GDDR5 FrameBuffer D0



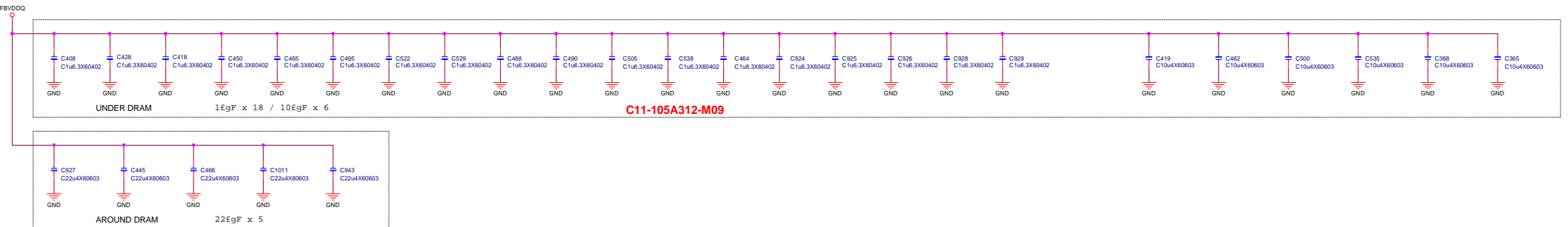
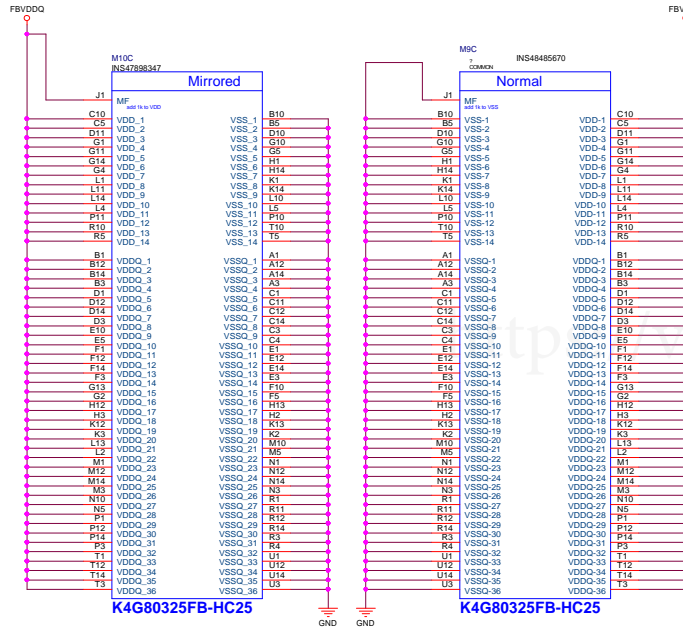
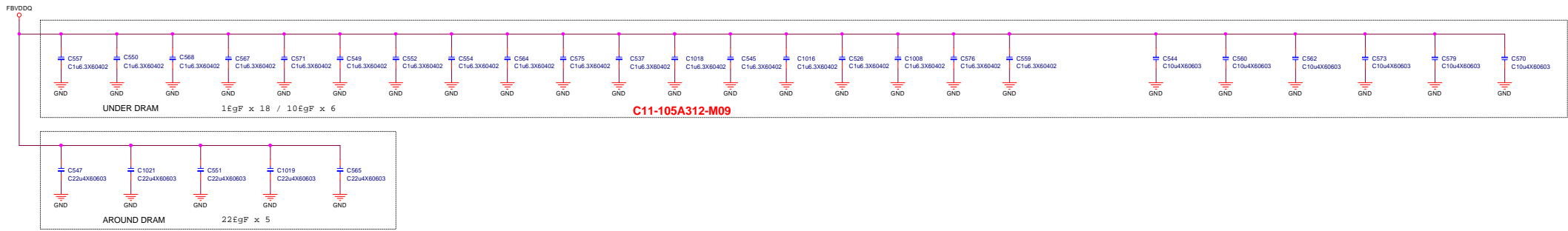
Title		
DGPU_GDDR5 FrameBuffer D0		
Size	Document Number	Rev
A3	MS-16P11	0A
Date:	Wednesday, May 03, 2017	Sheet 21 of 82

DGPU_GDDR5 FrameBuffer D1



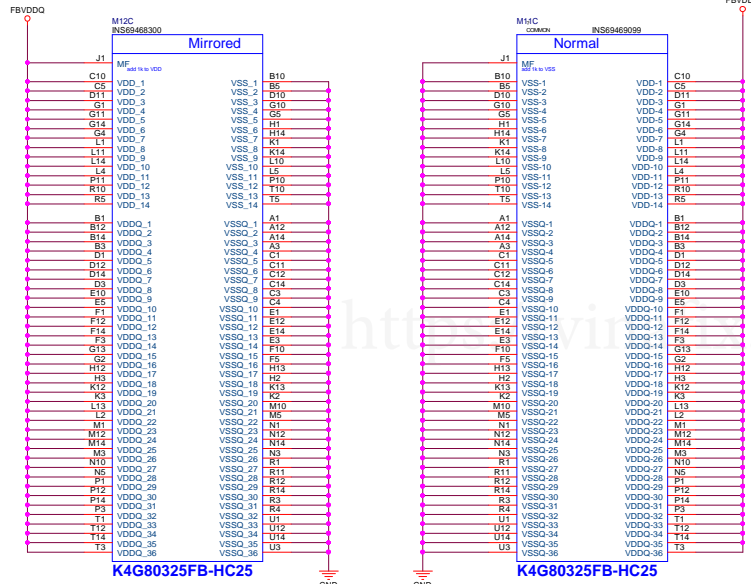
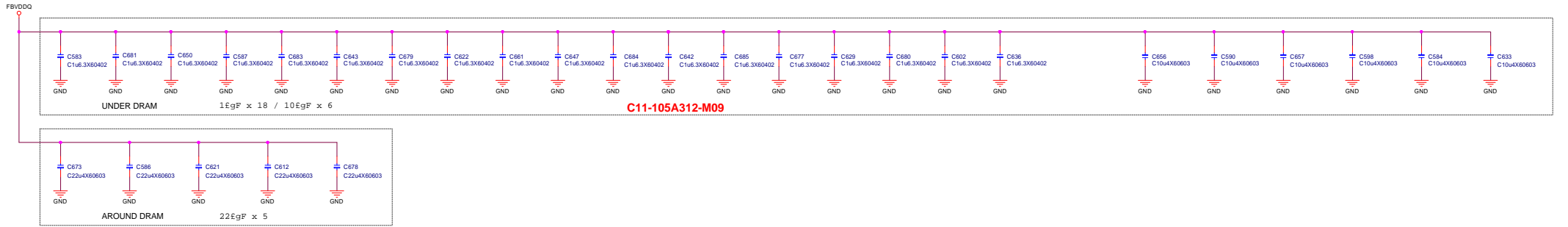
Title		
DGPU_GDDR5 FrameBuffer D1		
Size	Document Number	Rev
A3	MS-16P11	0A
Date:	Wednesday, May 03, 2017	Sheet 22 of 82

Frame Buffer Partition C Decoupling



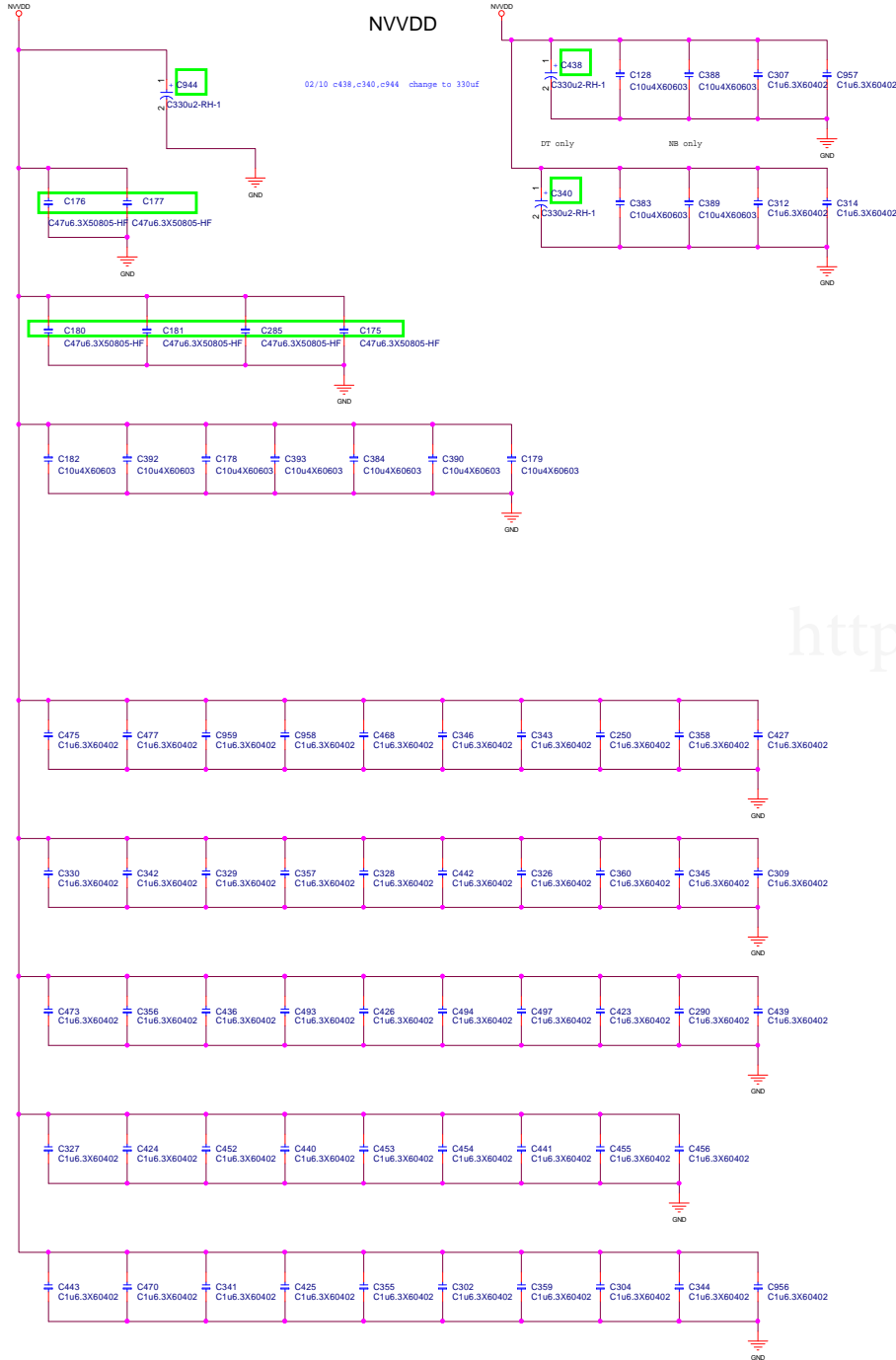
Micron PN : M12-2563215-M30 / MT51J256M32HF-80:A (256Mx32bit)
 Samsung PN : M12-8032535-S02 / K4G80325FB-HC25 (256Mx32bit)

Frame Buffer Partition D Decoupling

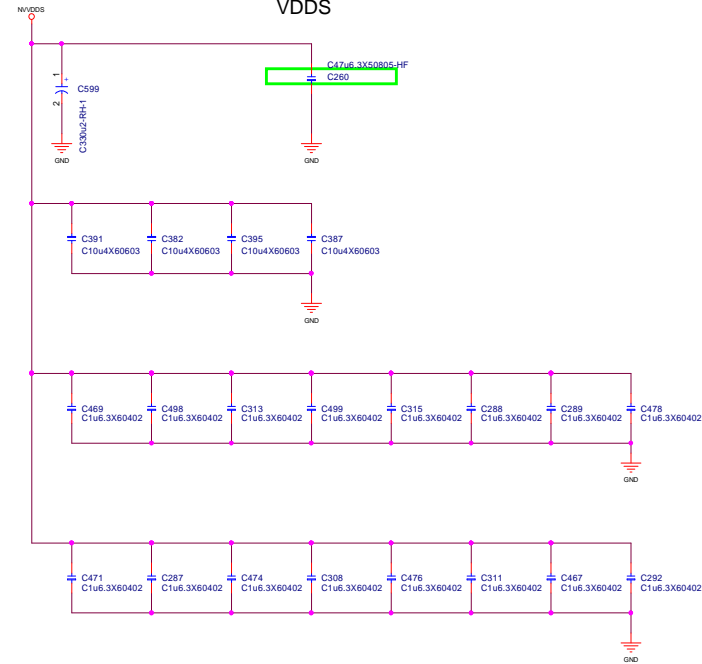


GPU DECOUPLING A

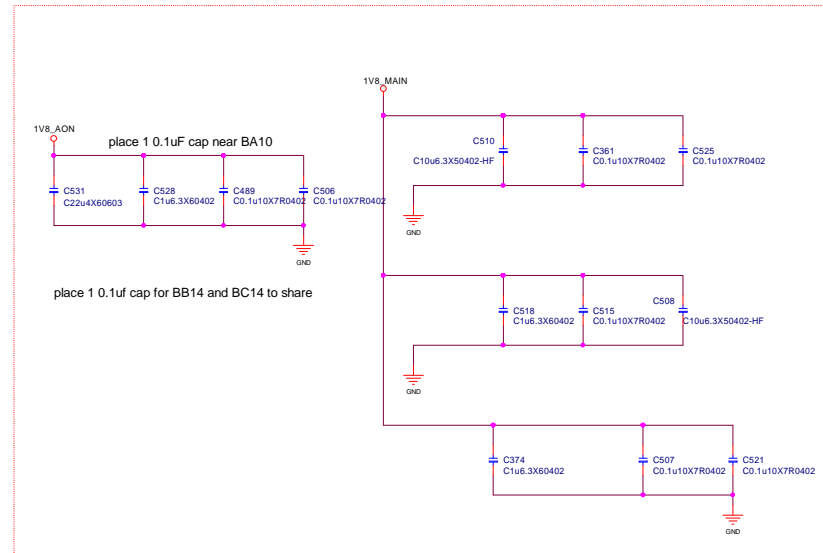
NVVD



VDDS



<https://vinafix.com>



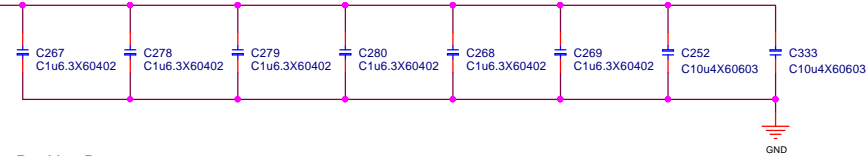
GPU DECOUPLING B

FBVDDQ

FBVDDQ

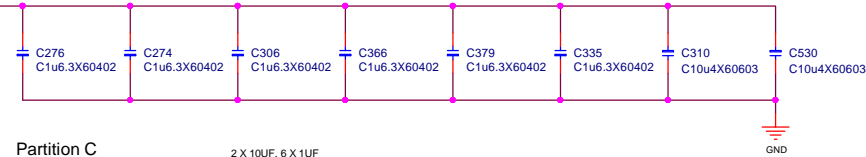
Partition A

2 X 10UF, 6 X 1UF



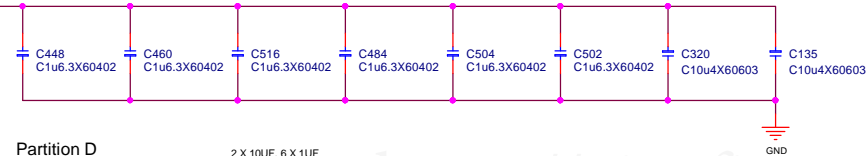
Partition B

2 X 10UF, 6 X 1UF



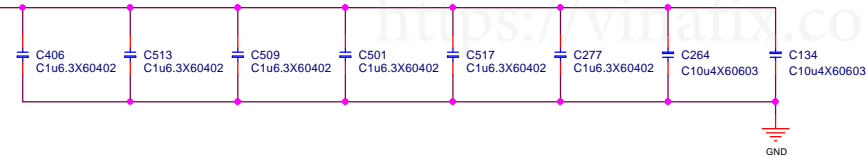
Partition C

2 X 10UF, 6 X 1UF



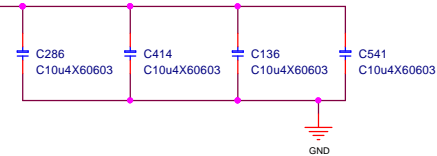
Partition D

2 X 10UF, 6 X 1UF



Place close to GPU

4 X 10UF

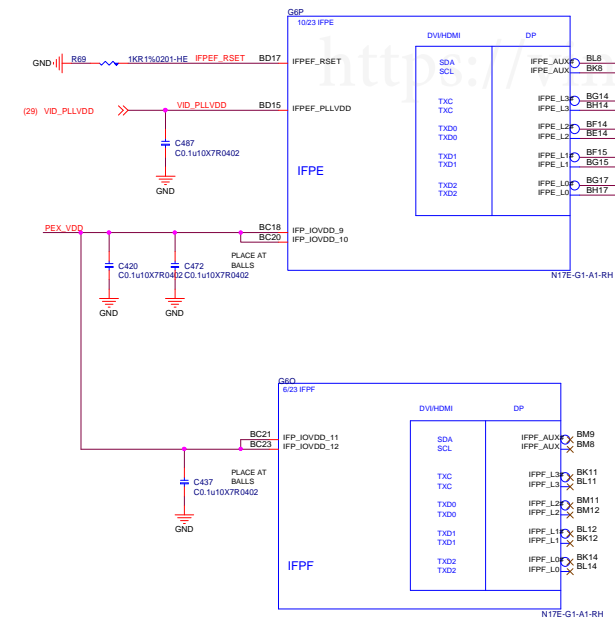
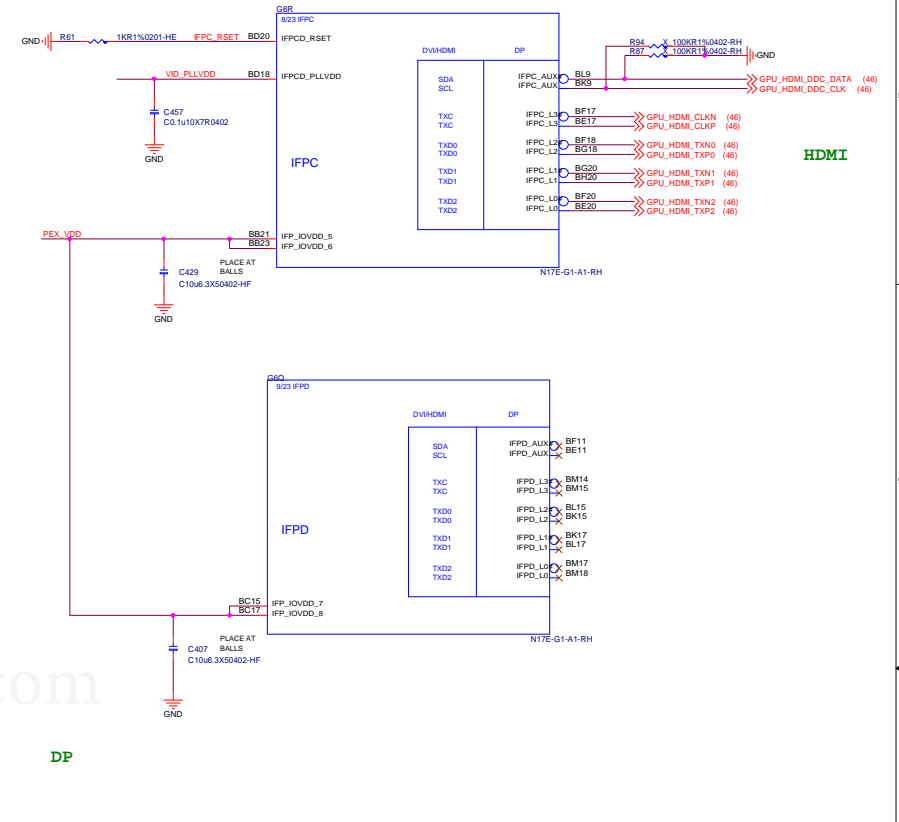
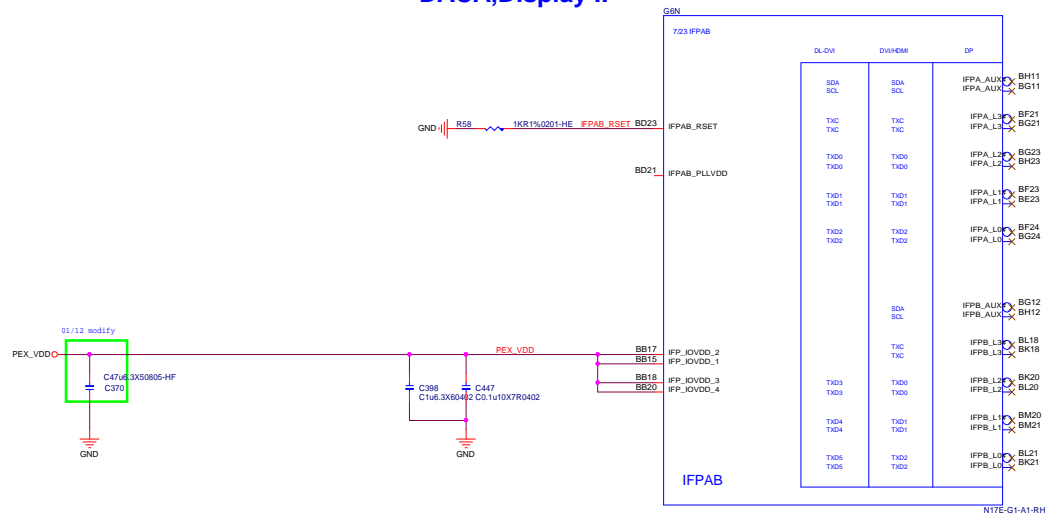


Place close to GPU

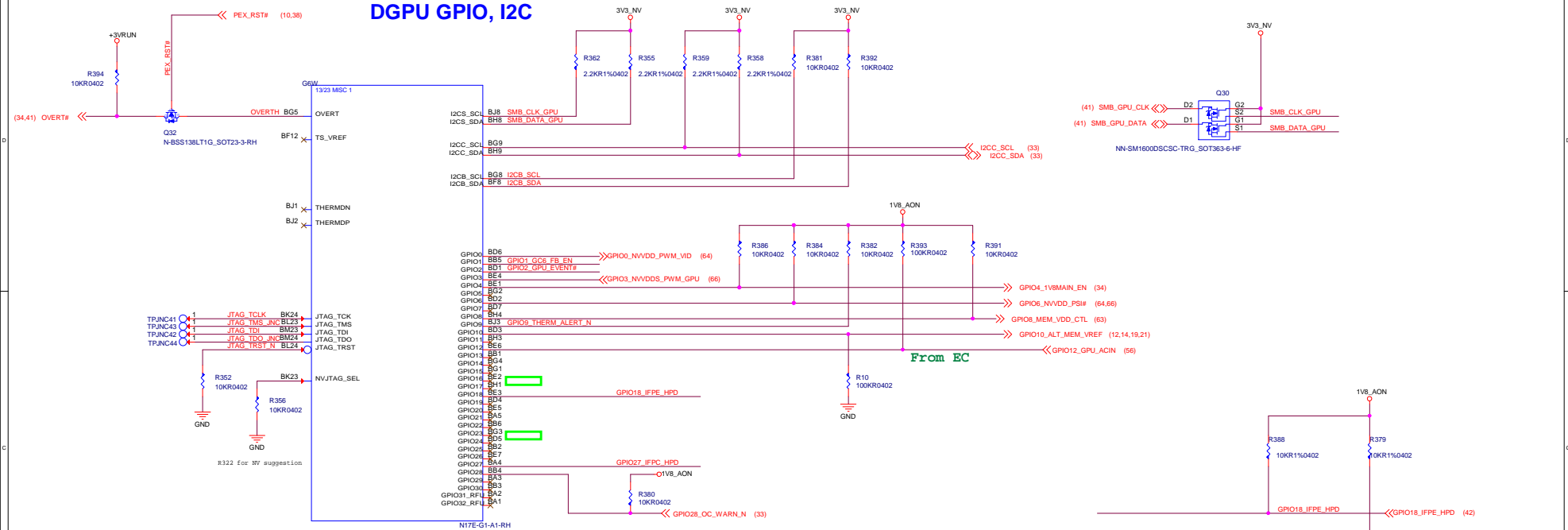
9 x 22UF



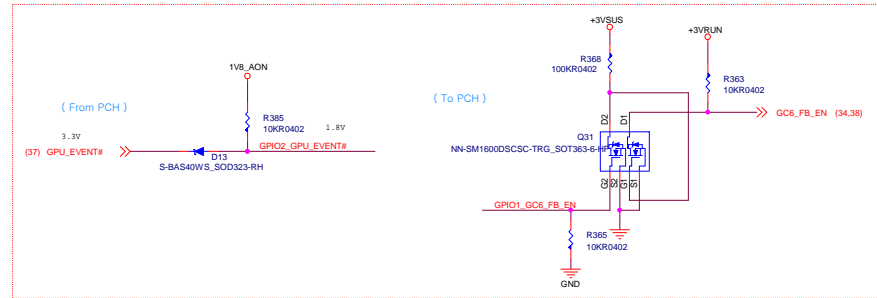
DACA,Display IF



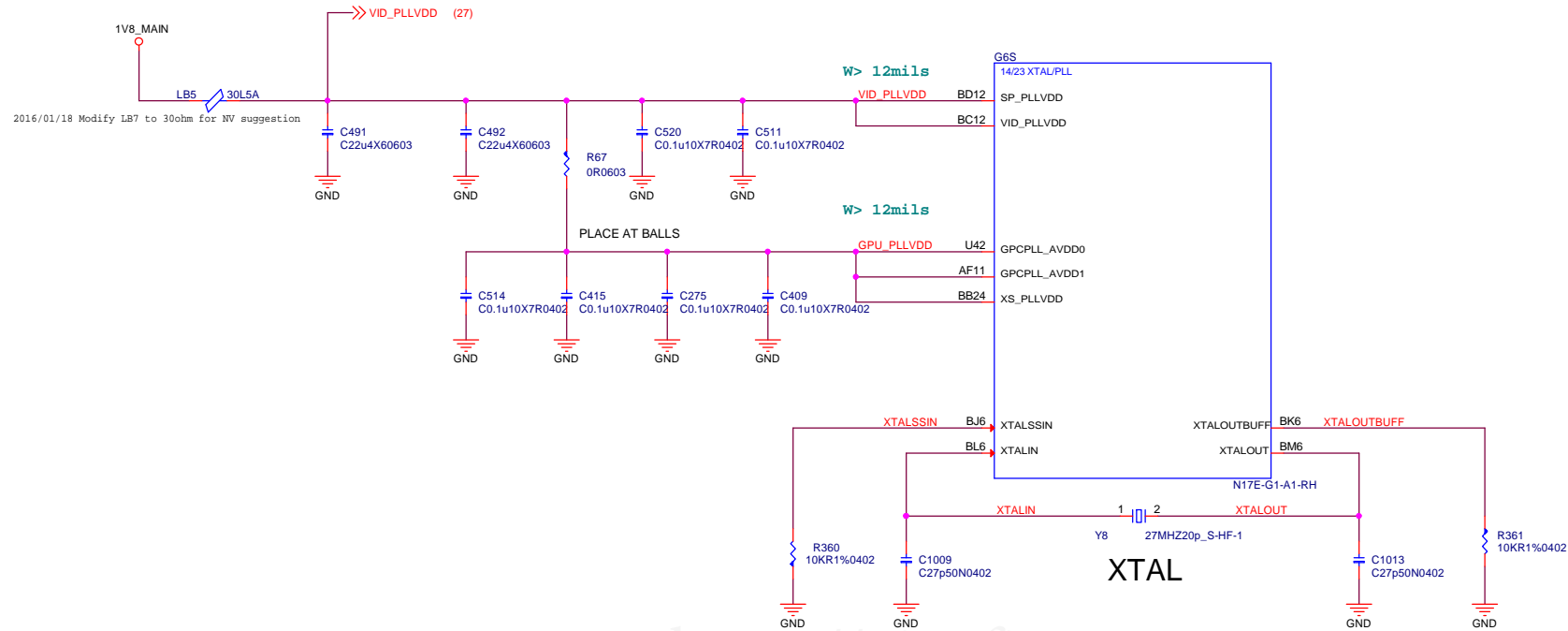
DGPU GPIO, I2C



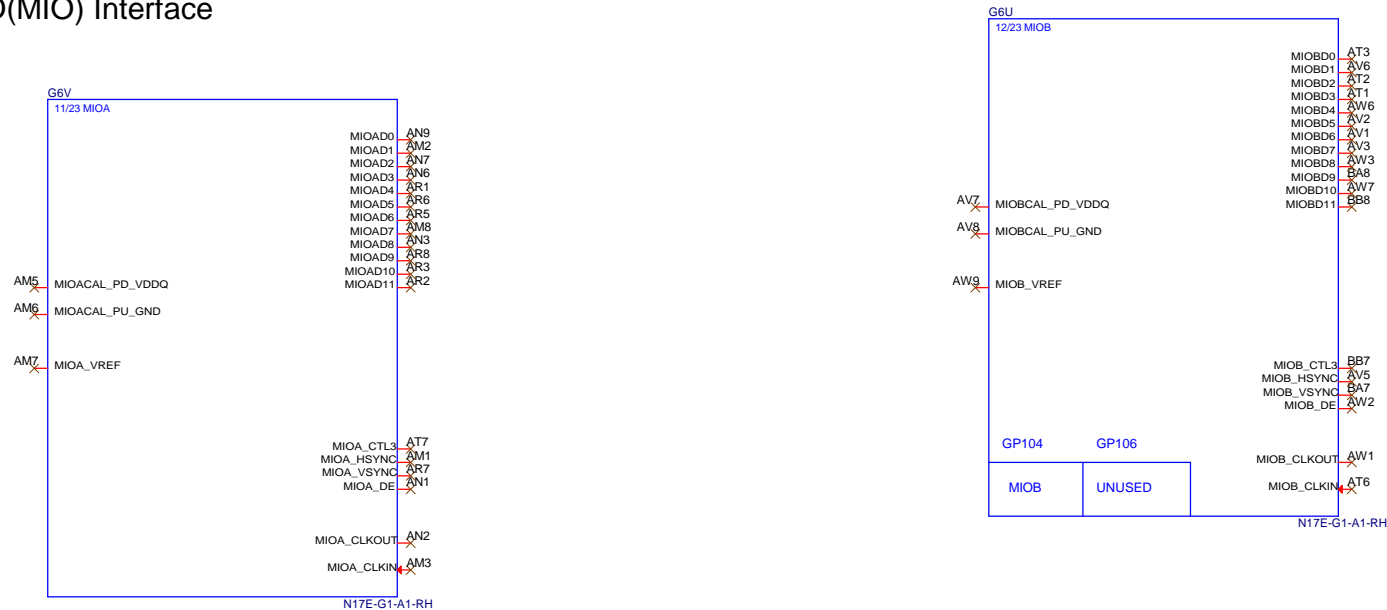
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8_AON
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	10K pull-up to 1V8_AON
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	10K pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Fram Lock	1V8 pull-up to 1V8_AON
GPIO6	PSI	O	Phase shedding	10K pull-up to 1V8_AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FB/IO/0 power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	I	System side PCI reset Monitor	10K pull-up to 3V3_AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3Dvision	O	3D Vision L/R signal	100K pull-down
GPIO20	NVVDD8_PSI GC5_MODE	O		
GPIO21	SLI_RASTER_SYNC	I	SLI Raster Sync	100K pull-down
GPIO22	SLI_SWAP_DRY	I	SLI Swap Ready	1K pull-up to 3V3_AON
GPIO23	GPU_PEX_RST_HOLD	O	GPU PCIe self-reset control	10K pull-up to 3V3
GPIO24	HPD_F	I	Hot Plug Detect for IFPDF	
GPIO25	RESERVED			
GPIO26	RESERVED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	
GPIO28	OC_WARN	I	Over current throttling	10K pull-up to 1V8_AON
GPIO29	EDPC_OUTPUT_CAP	I	Input from power supply	0 to 1V8
GPIO30	RESERVED			



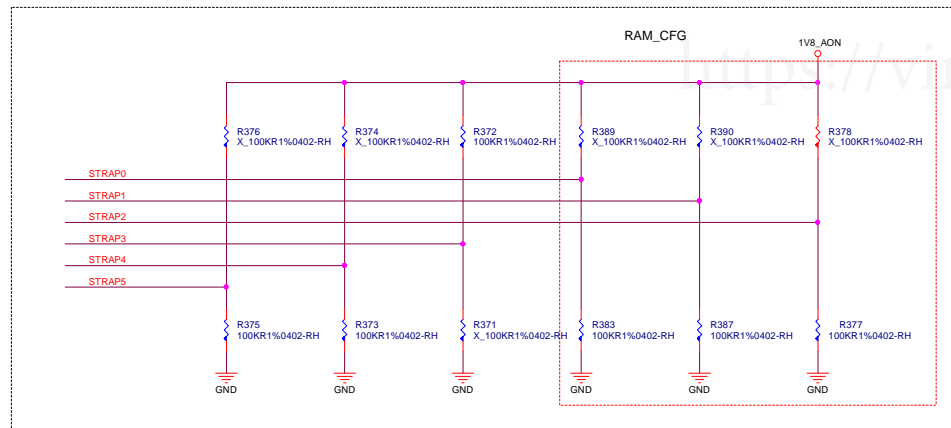
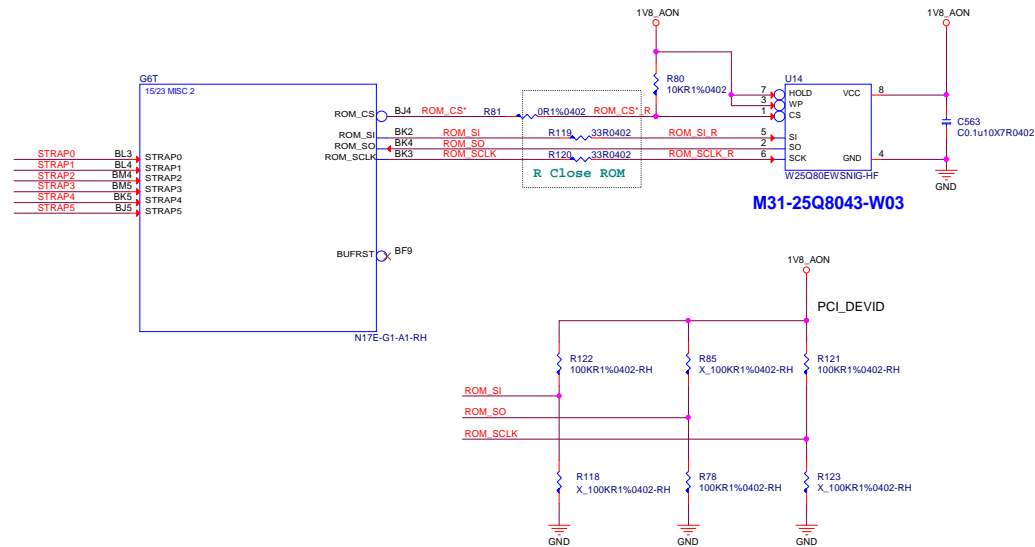
DGPU MIO & XTAL



Multi-use IO(MIO) Interface



ROM, MULTI-LEVEL STRAPS



DEFAULT SETTING	V_TOP1	5010
	<input checked="" type="checkbox"/> M12-8032535-S02	
	X_K4G80325FB-HC25	
	V_TOP2	5010
	<input checked="" type="checkbox"/> M12-2563215-M30	
	X_MT51J256M32HF-80:A	
	V_TOP3	5010
	<input checked="" type="checkbox"/> M12-5GC2H05-H23	
	X_H5GC2H24BFR-T2C	

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	V
L	L	H	00001	V
L	H	L	00010	
L	H	H	00011	
H	H	L	00110	
H	H	H	00111	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

SAMSUNG 0X0
MICRON 0X1
HYNIX 0X2

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

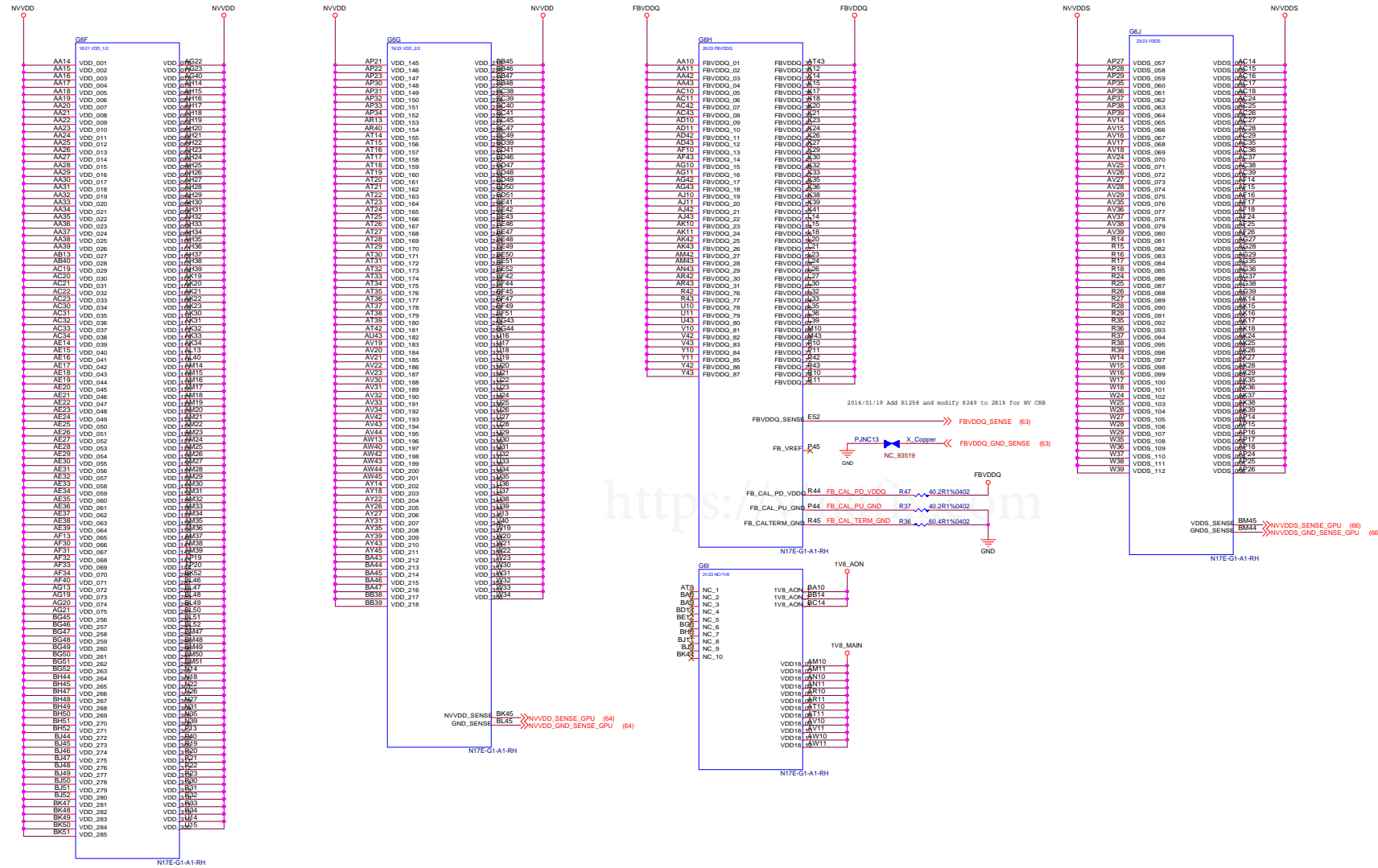
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

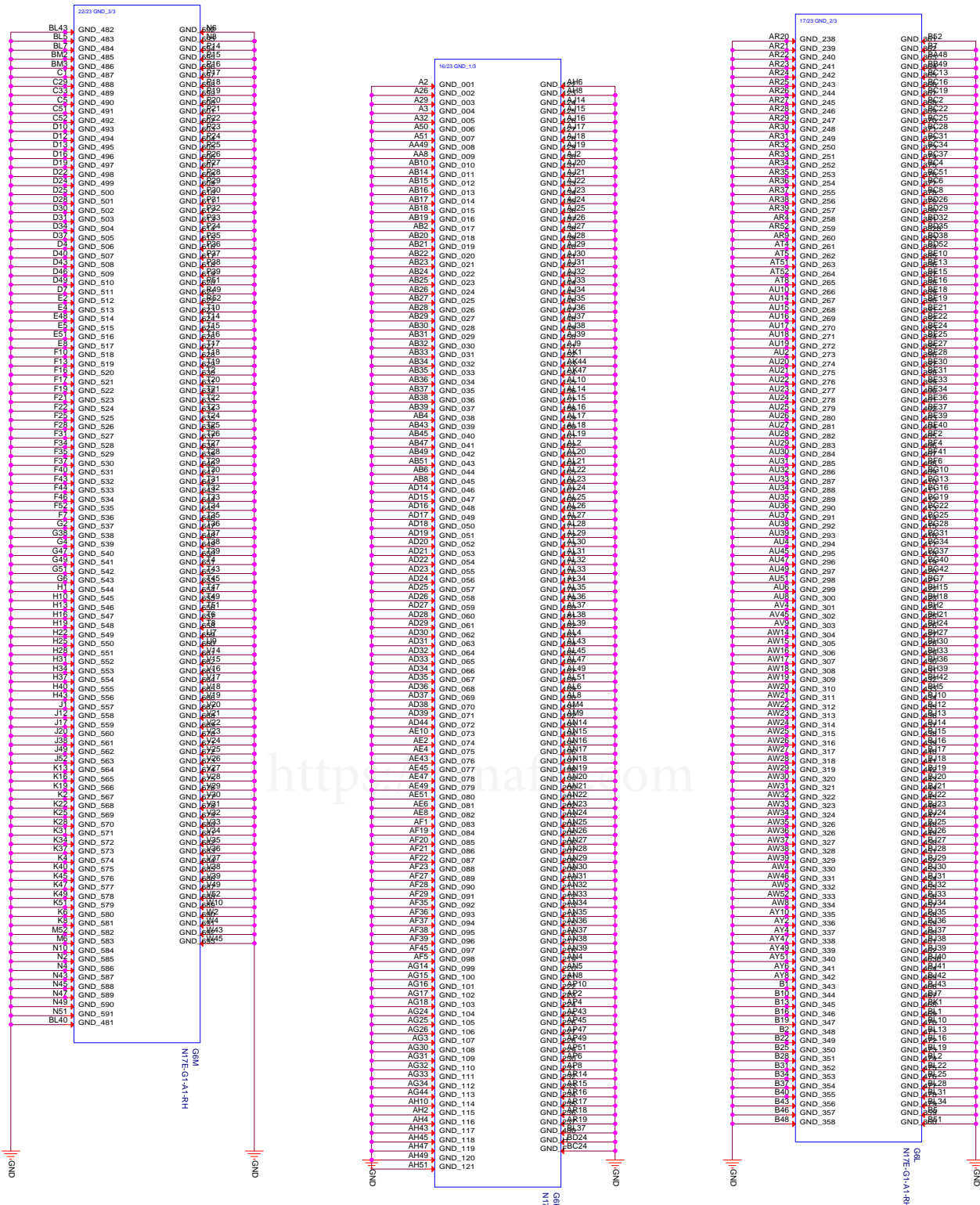
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

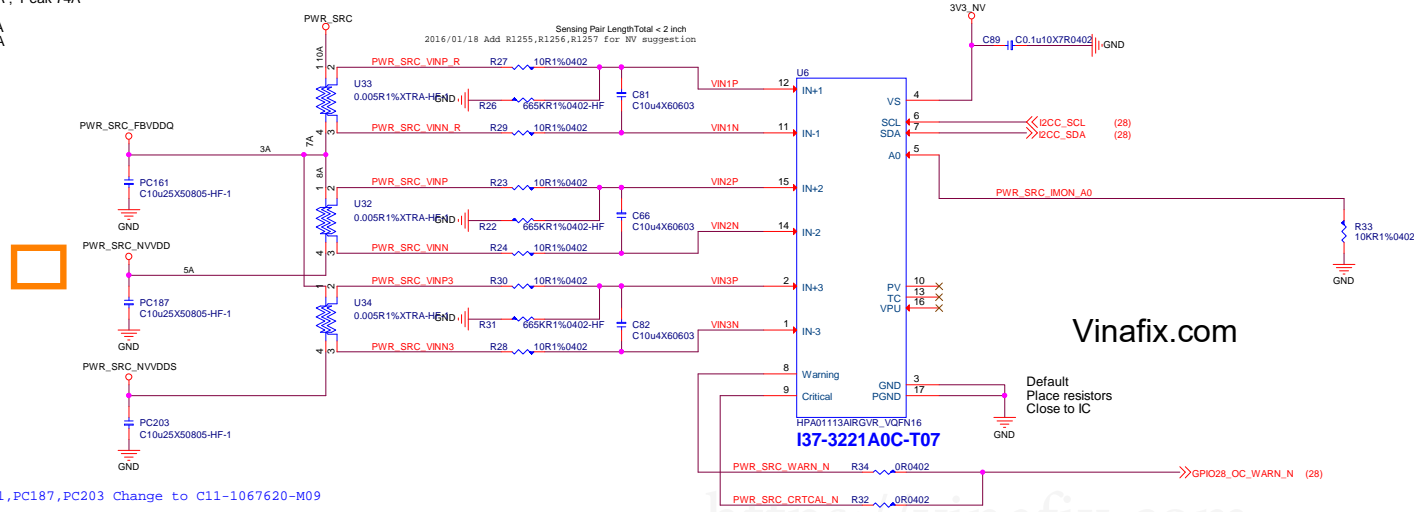
GPU NVVDD, FBVDDQ





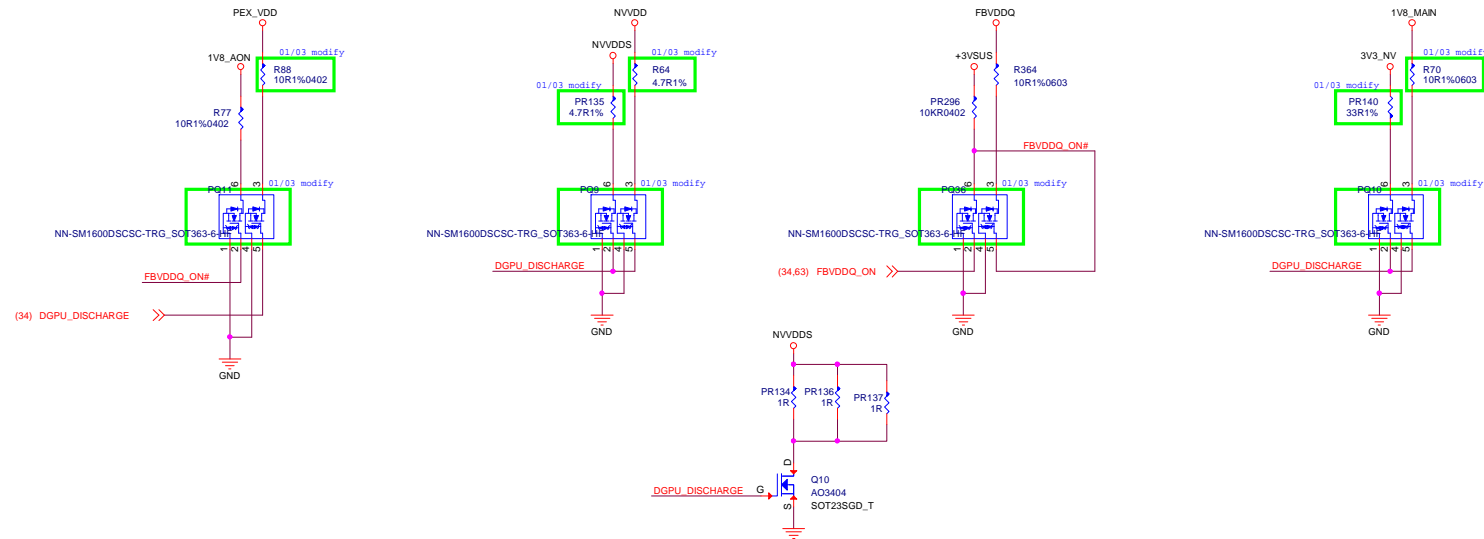
DGPU_Power Control

EDP Design Guide:
N17E-G1(90W)
NVVDD : 58A ; Peak 136A
NVVDDS : 28A ; Peak 74A
1.8V : 0.9A
PEX_VDD : 3A
FBVDDQ : 16A



04/07 1.0 PC161,PC187,PC203 Change to C11-1067620-M09

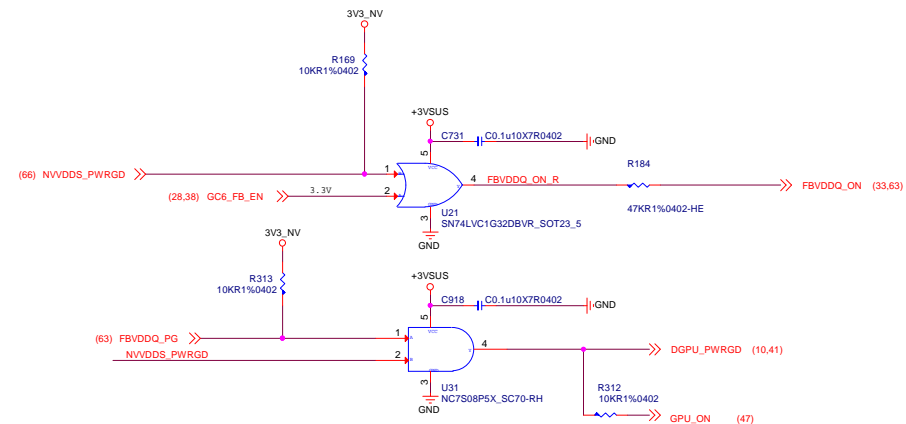
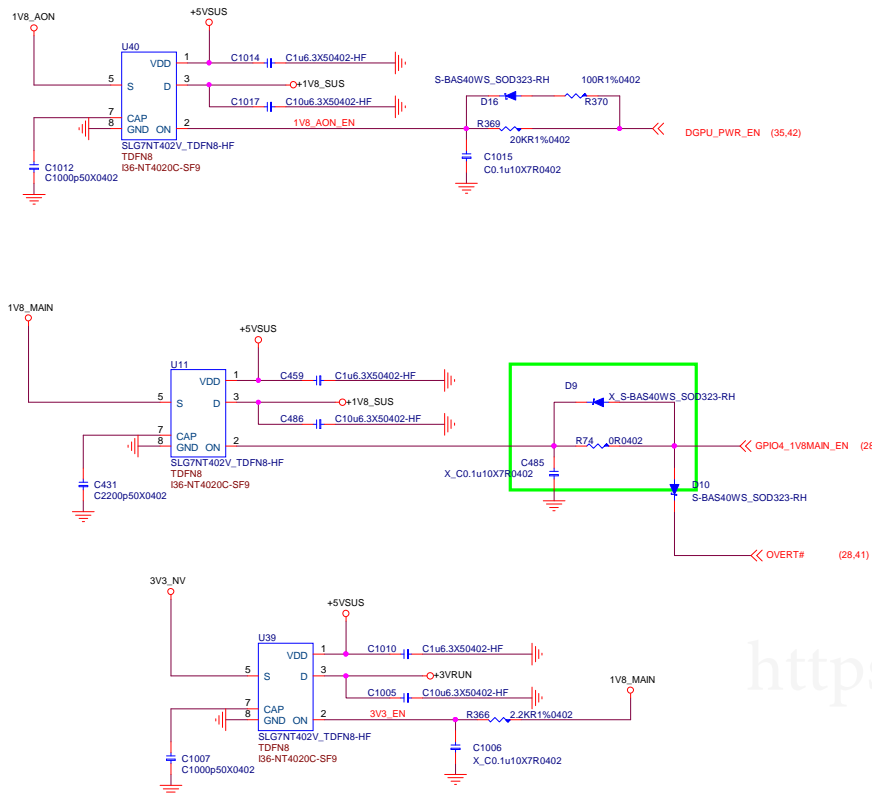
Discharge



msi MICRO-STAR INT'L CO.,LTD.	
File DGPU Power Control	
Size Custom	Document Number MS-16P11
Date Wednesday, May 03, 2017	Sheet 33 of 82
Rev 0A	

nVIDIA Power Sequence Power UP

Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV -> NVVDD -> NVDDS/PEX_VDD -> FBVDDQ -> DGPUPWRGD

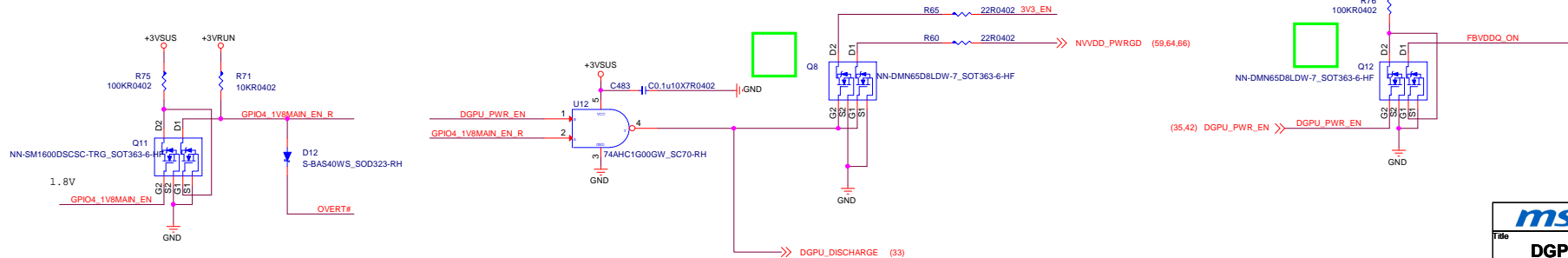


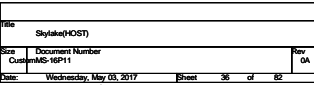
<https://vinafix.com>

nVIDIA Power Sequence Power Down

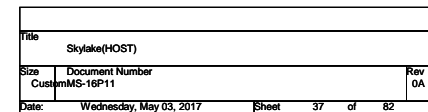
Power down = FBVDDQ -> NVDDS/PEX_VDD -> 3V3_NV -> 1V8_AON -> 1V8_MAIN

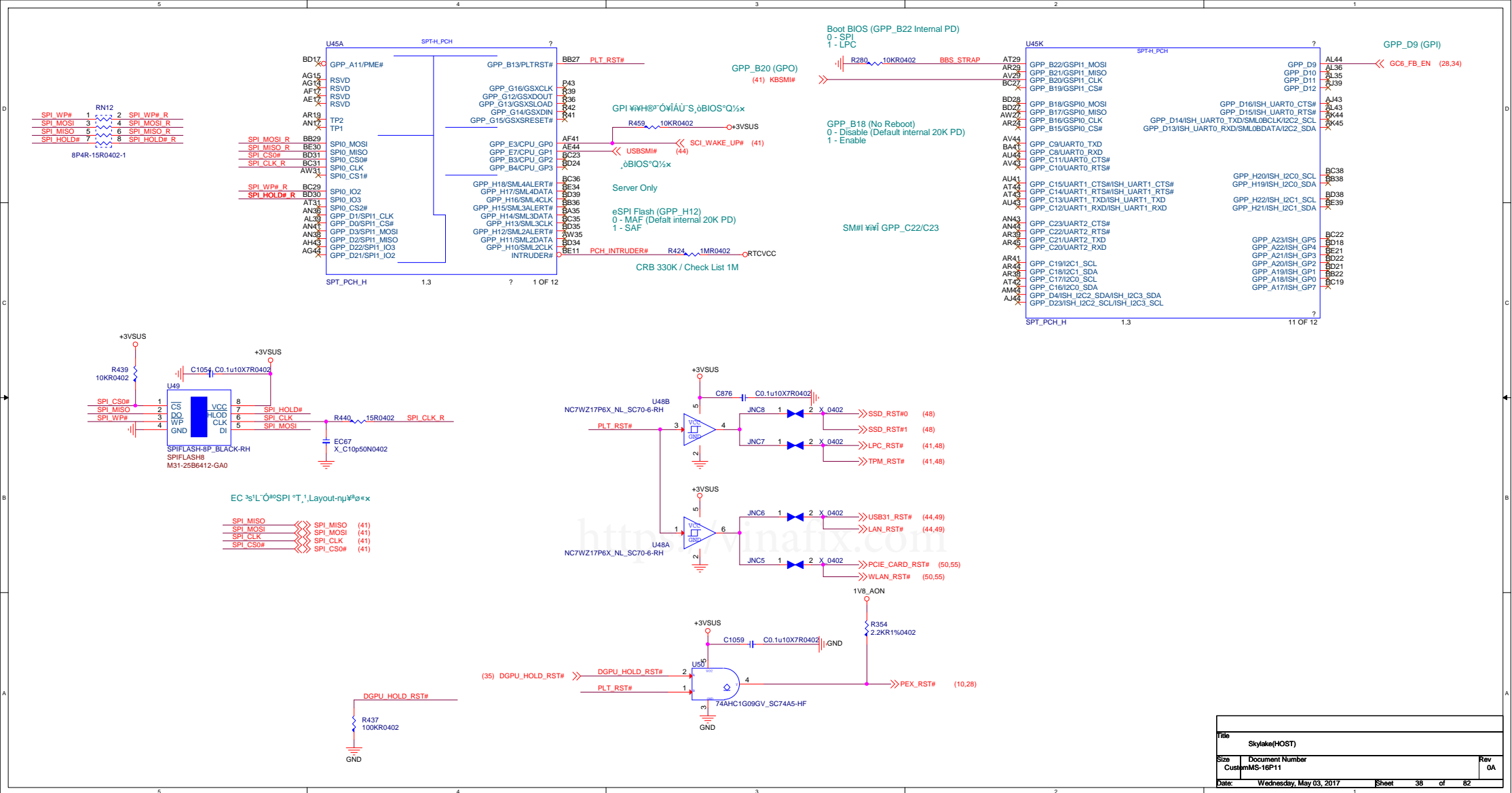
02/22 Q8,Q12 change to D03-65D8L09-D07





PCH EDS Page 52





LED Keyboard Pin Define

Pin	Define
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G

[illegible]

03/24 1.0 modify SCL3,SDA3
04/06 1.0 Add R619,R620,L28,L29,C1110

02/09 0B Add CN17

The schematic diagram for the NUMLED circuit shows a +5VRLIN input. This input is connected to a network of resistors and LEDs. Specifically, the input goes through a series of resistors (R62, R66, R19, R14) and LEDs (LED6, LED5). The circuit includes two LEDs (LED7 and LED6) in parallel, followed by a series LED (LED5). The output is connected to a MOSFET (Q6) which drives the NUMLED. The MOSFET is an NN-DMN65D8LDW-7_SOT363-6-HF. The circuit is labeled KB_NUMLED and includes a ground connection.

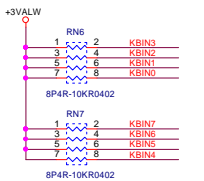
KBC/EC/uP (ENE9028)

Hardware Reset

PU/PD



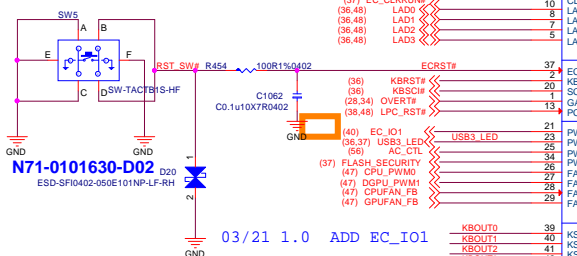
KB pull Hi 10k



+3VALW LID pull hi 10K



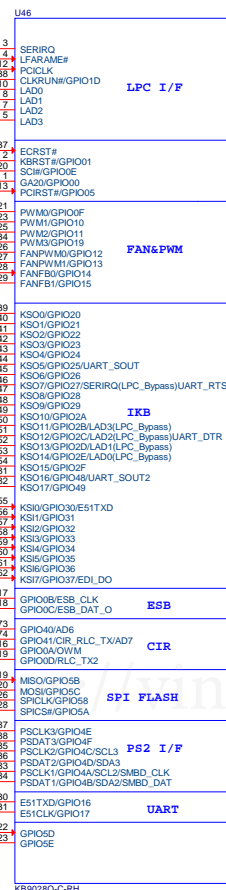
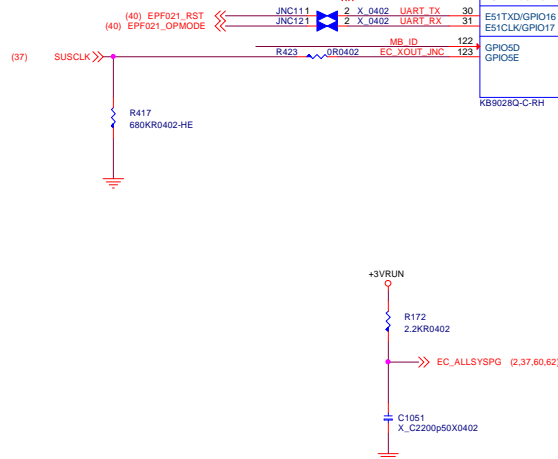
+3VALW



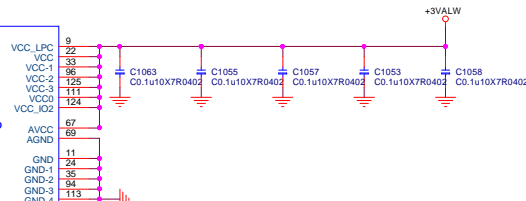
N71-0101630-D02 D20

03/21 1.0 ADD EC IO1

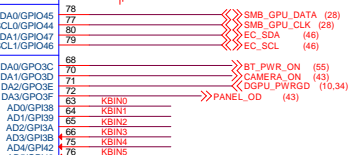
03/24 1.0 modify SCL3.SDA3



POWER/GROUND



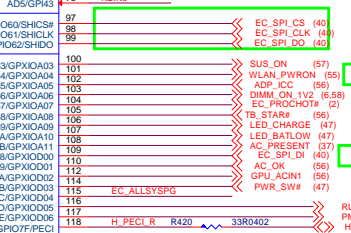
SMBUS | EDI | S



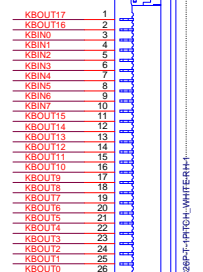
AD/DA



555

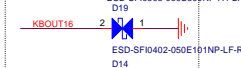
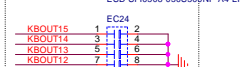
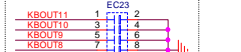
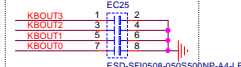
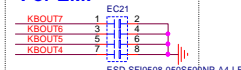


LED

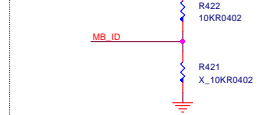


N5A-26F0270-A81

For EMI

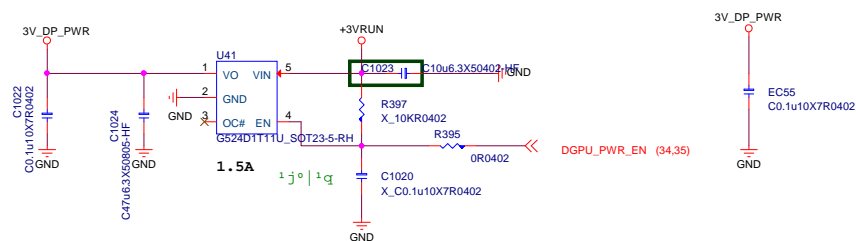


MotherBoard ID

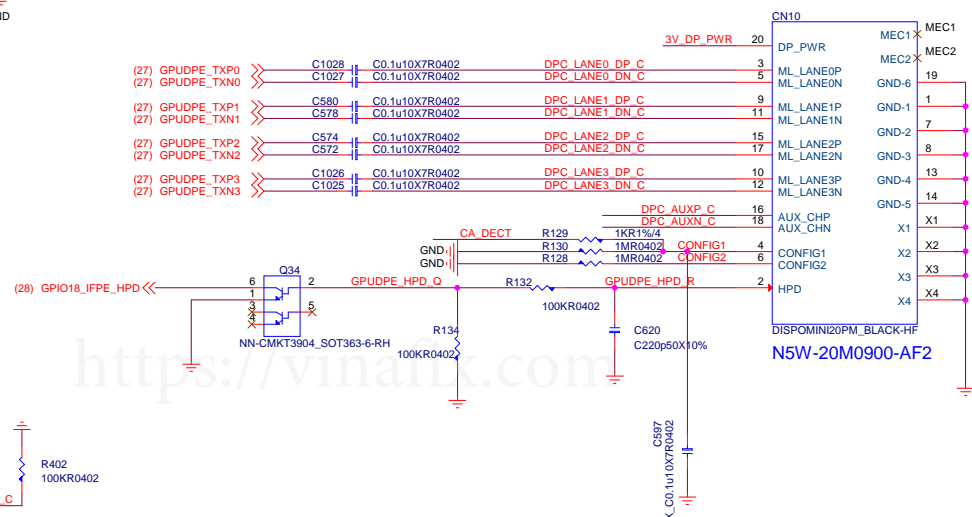


Display Port

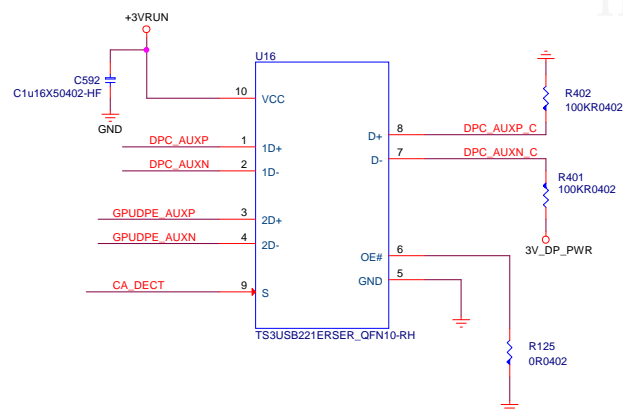
The preset trip limit must not exceed 3A at the Upstream device connector DP_PWR pin and 1.5A at the Downstream device connector DP_PWR pin.



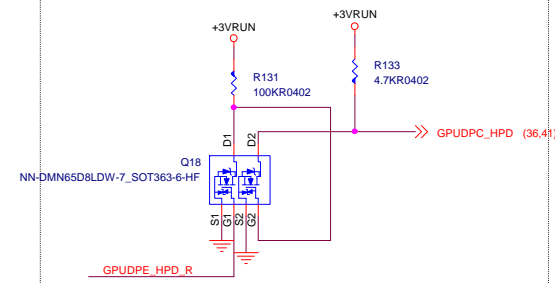
Display Port



DP/TMDS mode select



Level Shift 5V to 3V



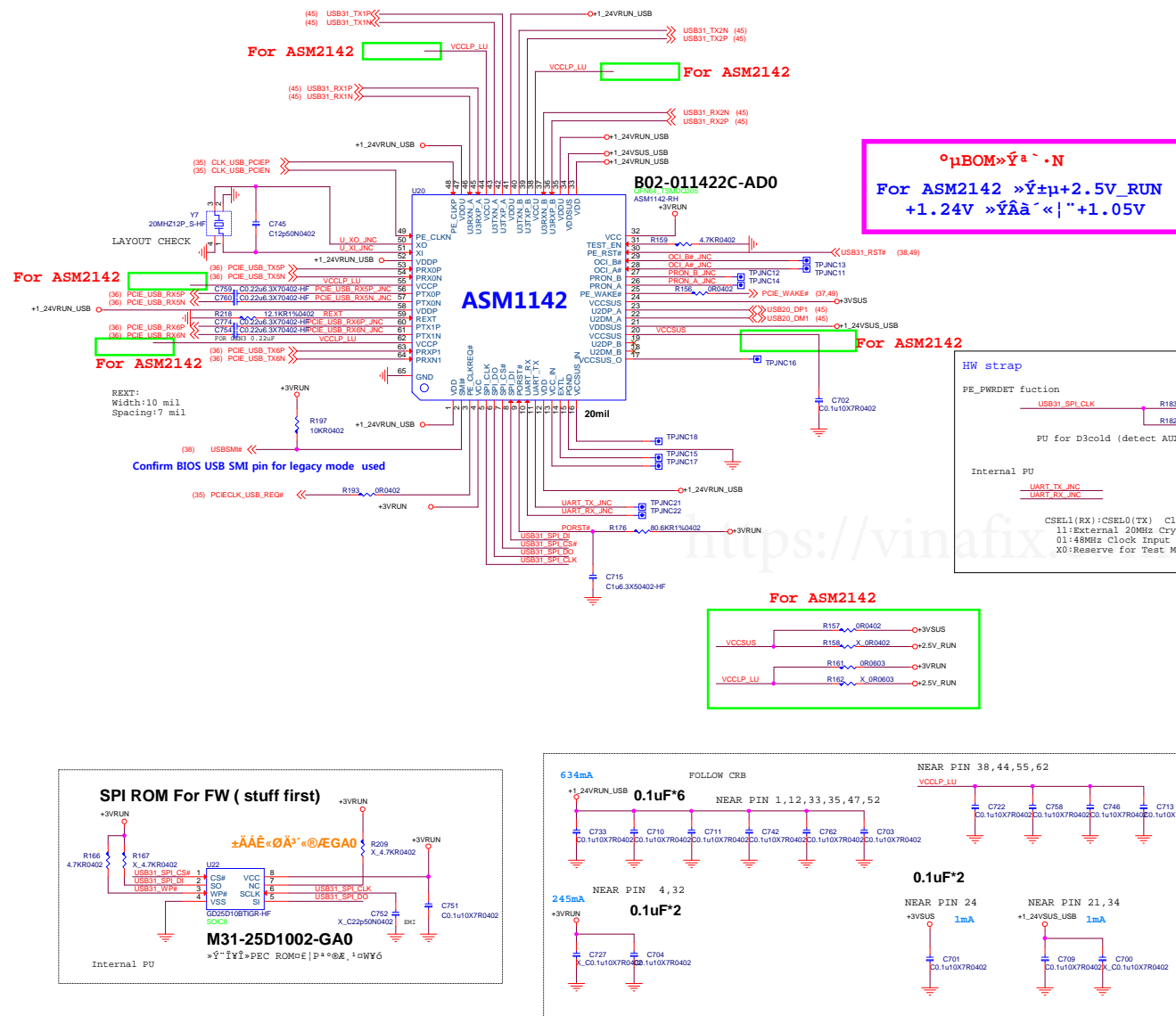
TS3USB221A TRUTH TABLE

S	OE#	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

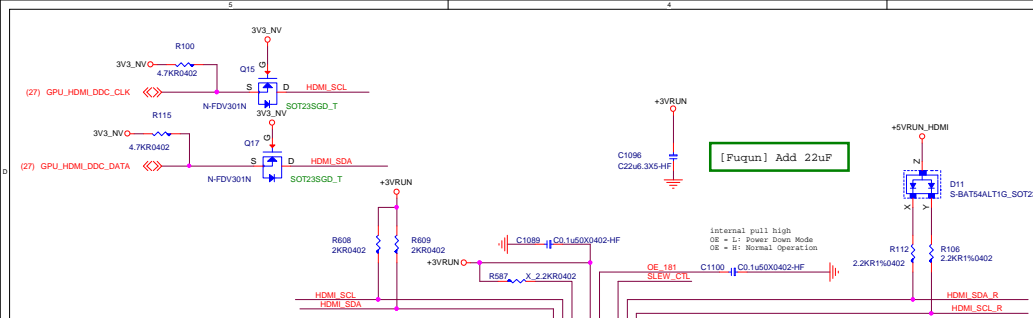
PCIE to USB 3.1

USB 3.0/ USB.3.1

Vinafix.com



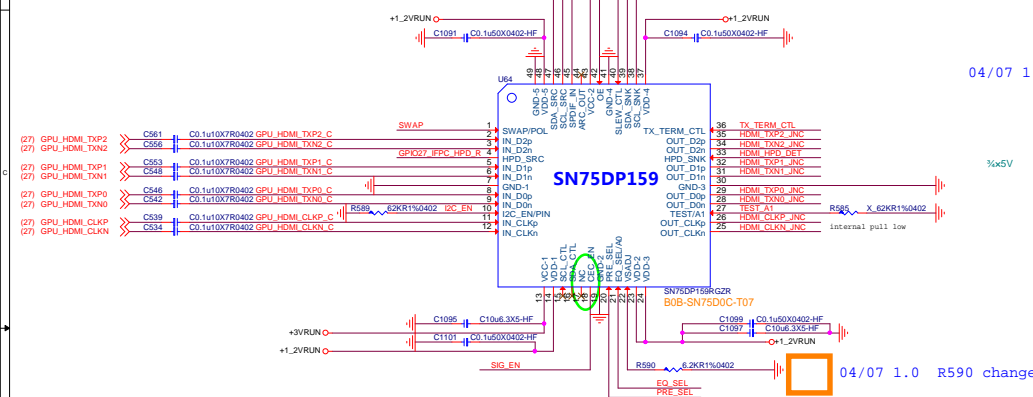
Title				
Skylake(HOST)				
Size	Document Number			Rev
Custom	MS-16P11			QA
Date:	Wednesday, May 03, 2017	Sheet	45	of 82



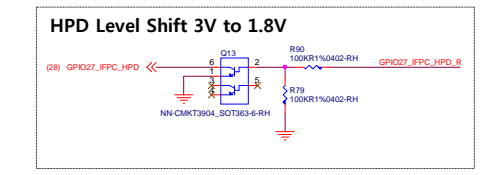
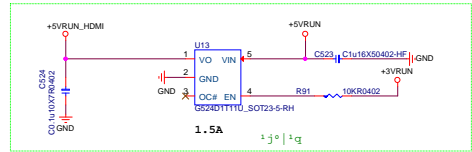
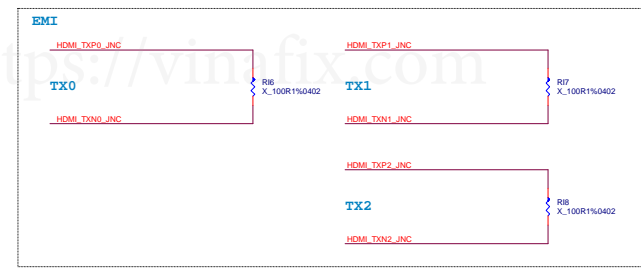
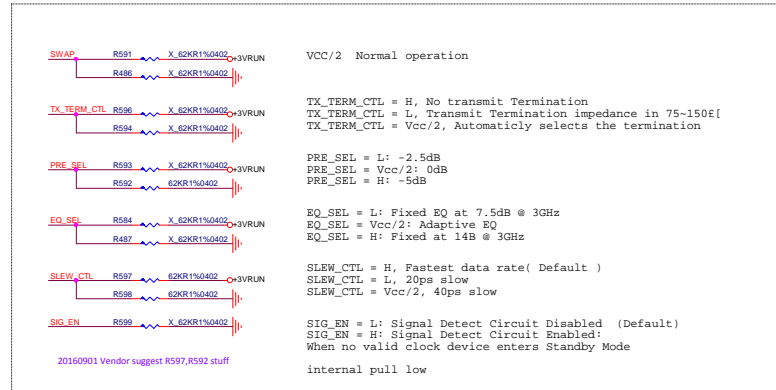
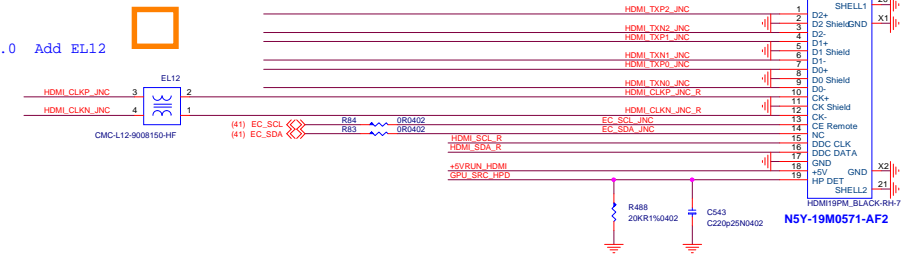
HDMI connector

An HDMI Source shall have +5V Power signal over-current protection of no more than 0.5A.

HPD_SNK Internal PD 150kohm

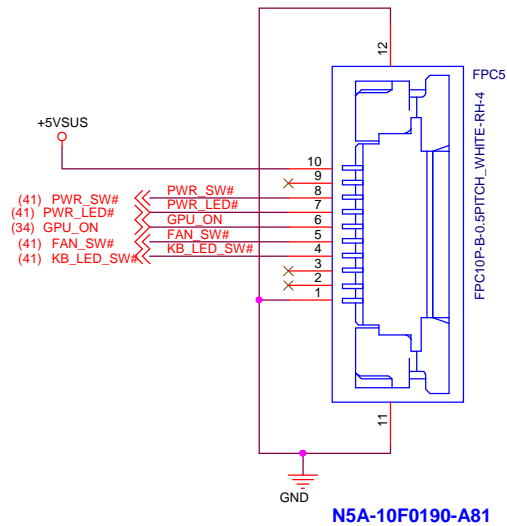


04/07 1.0 Add EL12

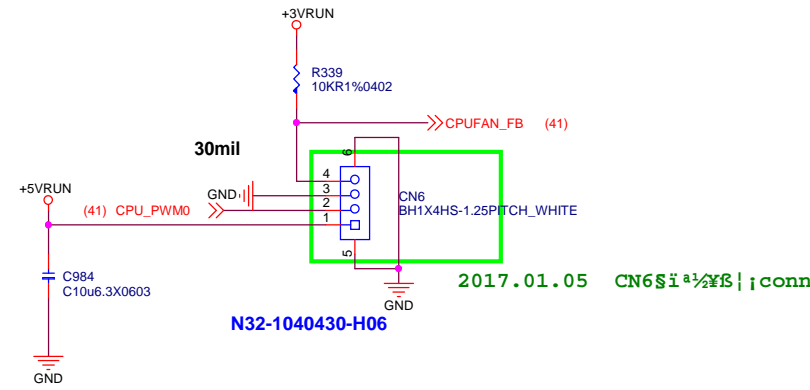


CPU FAN/CPU FAN/POWER CONN/ LED CONN

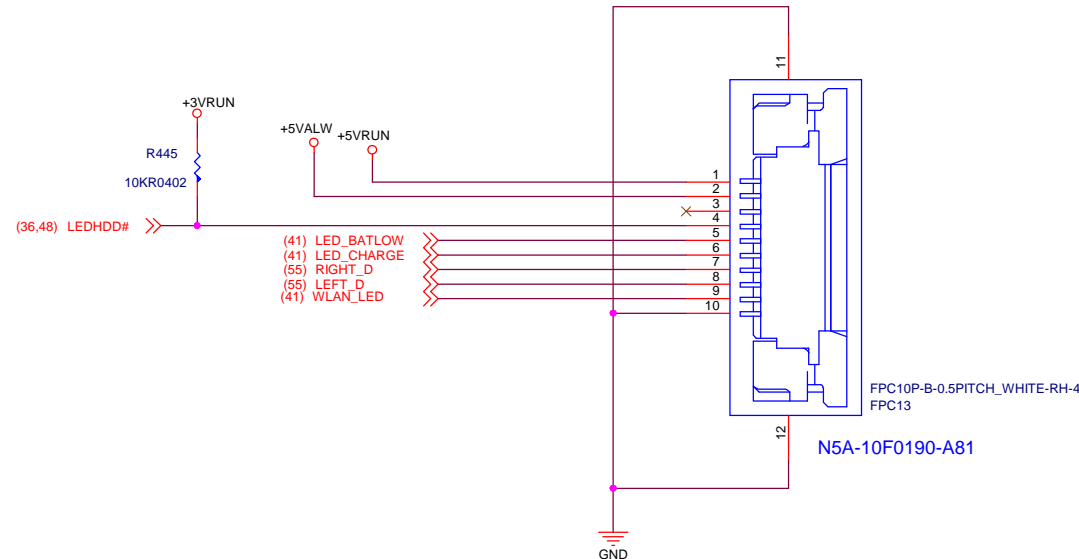
Power Switch Connector



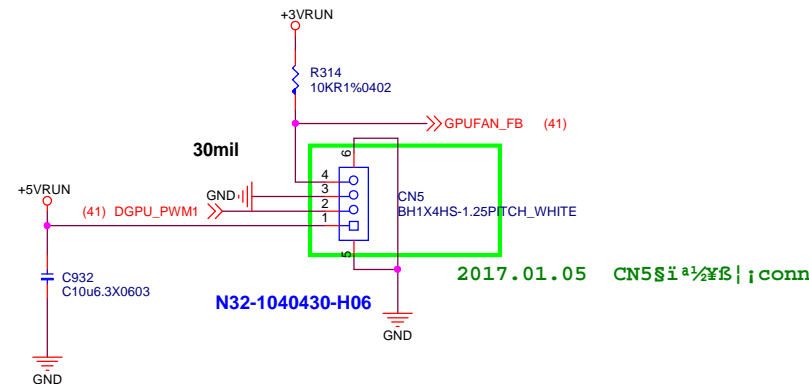
CPU FAN



Switch connector

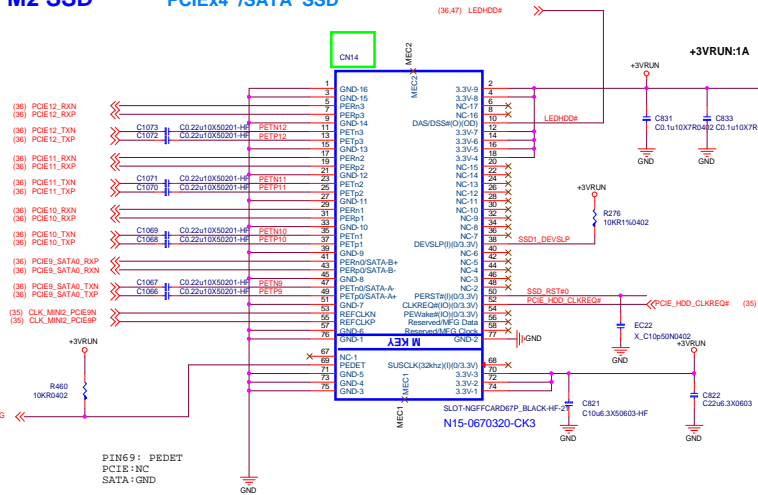


DGPU FAN



M2 SSD

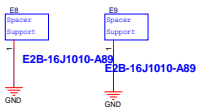
PCIEx4 /SATA SSD



Vinafix.com

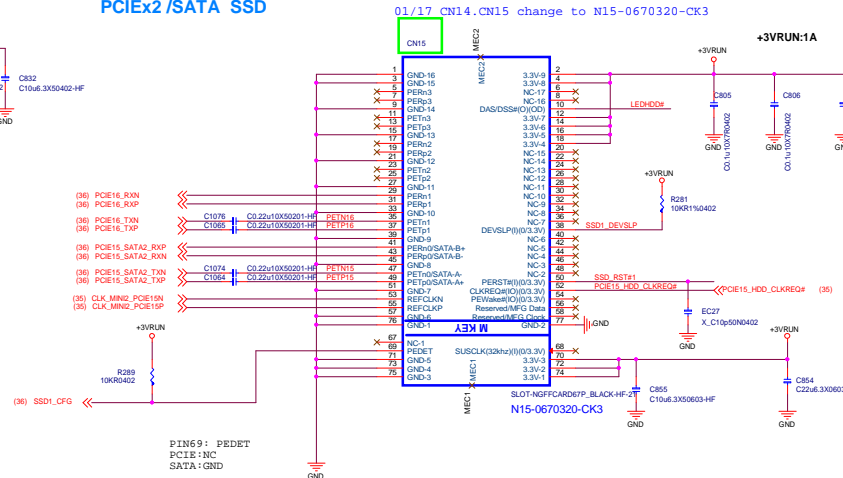
(38) SSD_RST#0 >> SSD_RST#0
(38) SSD_RST#1 >> SSD_RST#1

40	NC	No Connect
41	SATA-B+/PERn0	Host receiver differential signal pair
42	NC	No Connect
43	SATA-B-/PERp0	Host receiver differential signal pair
44	NC	No Connect
45	GND	Ground
46	NC	No Connect
47	SATA-A-/PETn0	Host Transmitter differential signal pair
48	NC	No Connect
49	SATA-A+/PETp0	Host transmitter differential signal pair



M2 SSD

PCIEx2 /SATA SSD

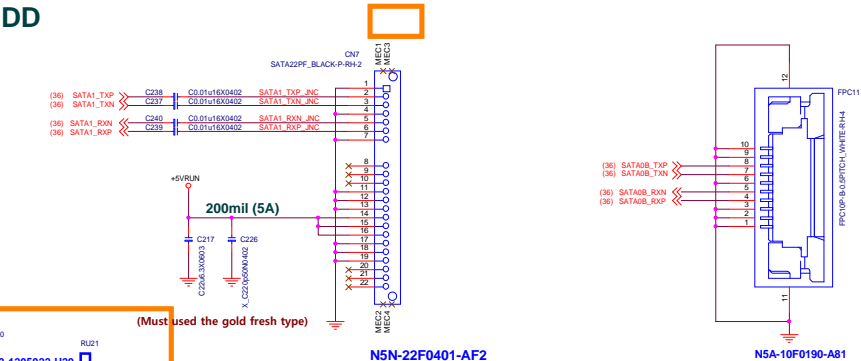


PIN69: PEDET
PCI-E: NC
SATA: GND

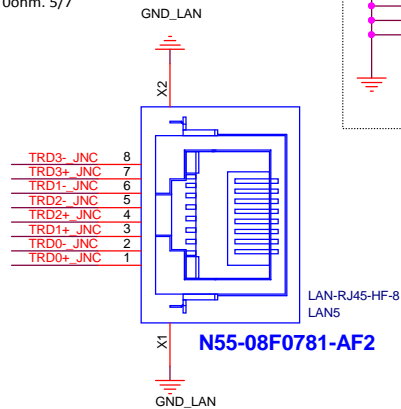
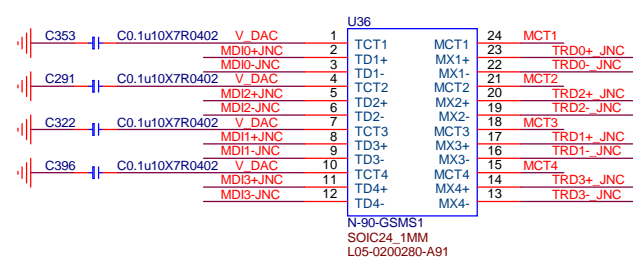
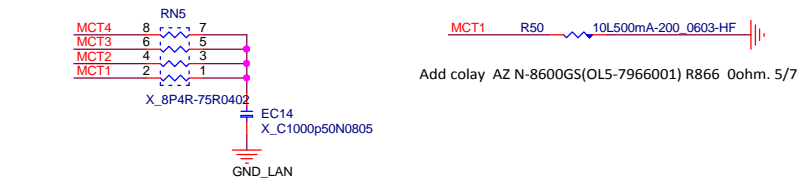
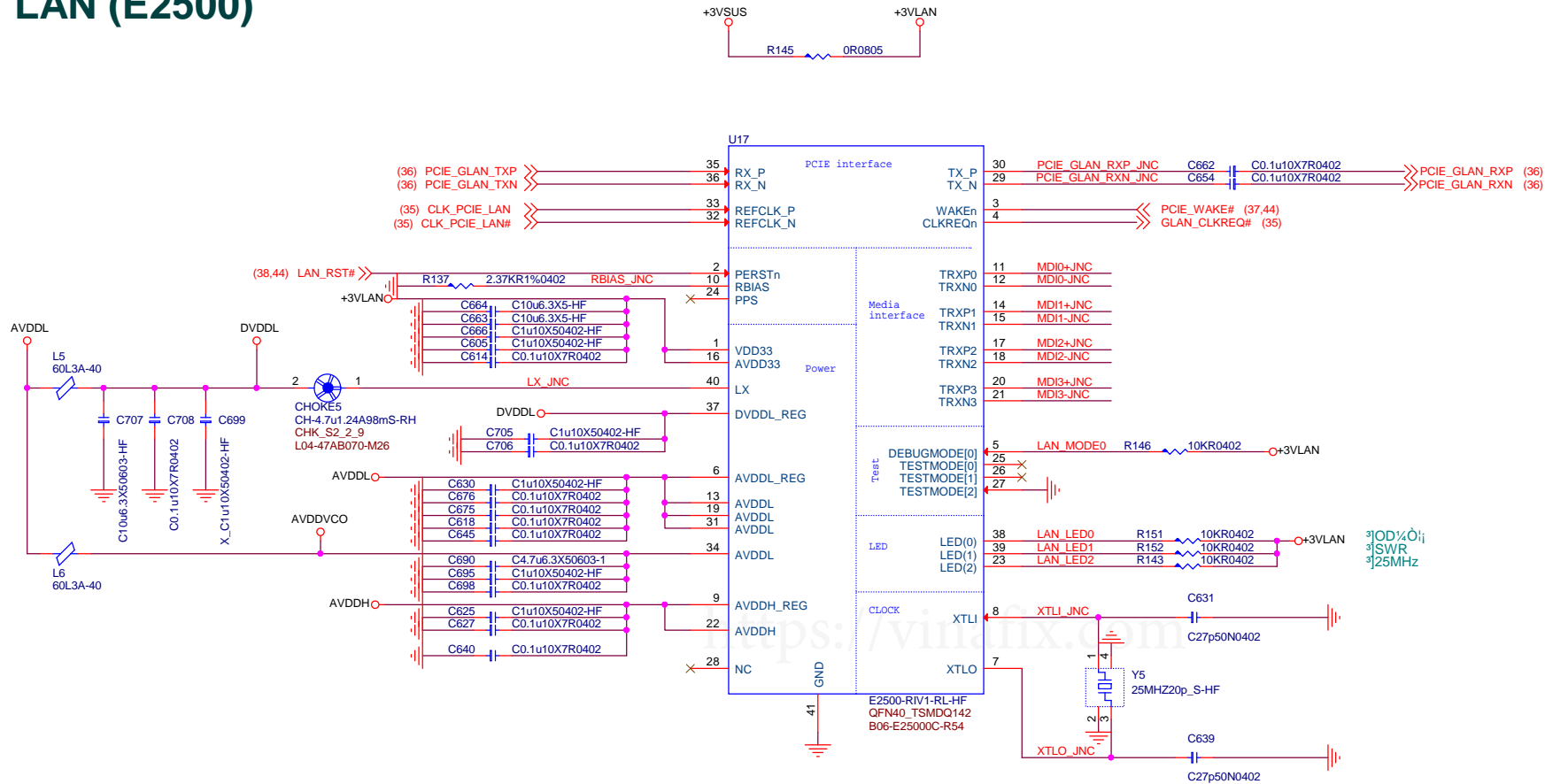
https://vinafix.com

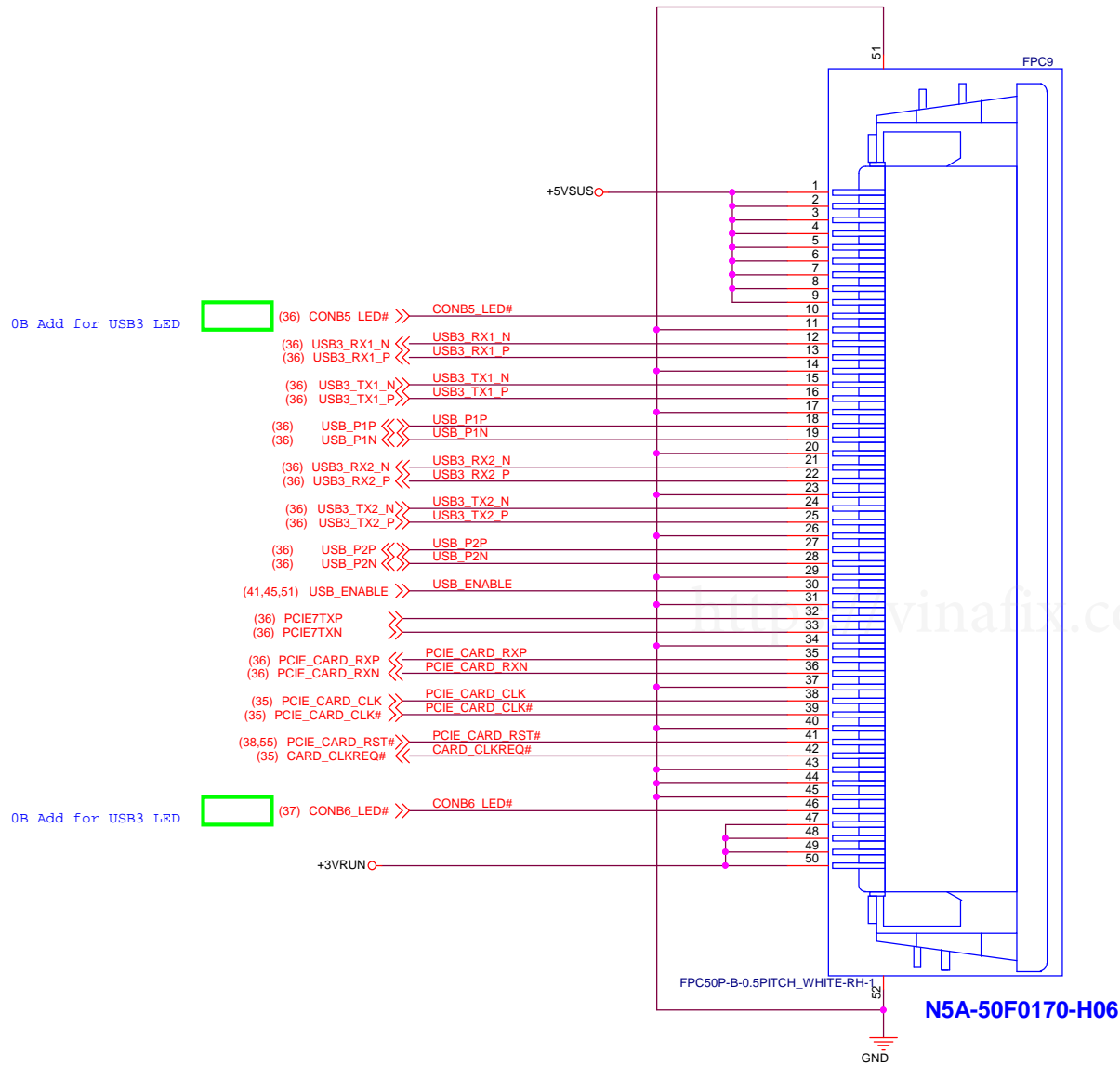
HDD

03/21 1.0 CN7 change to N5N-22F0401-AF2

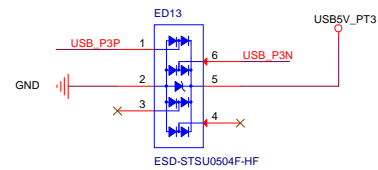
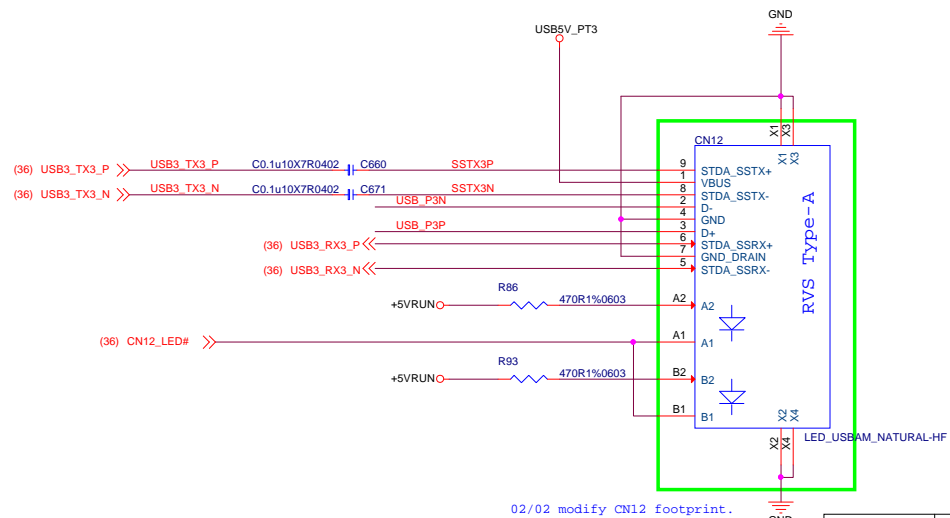
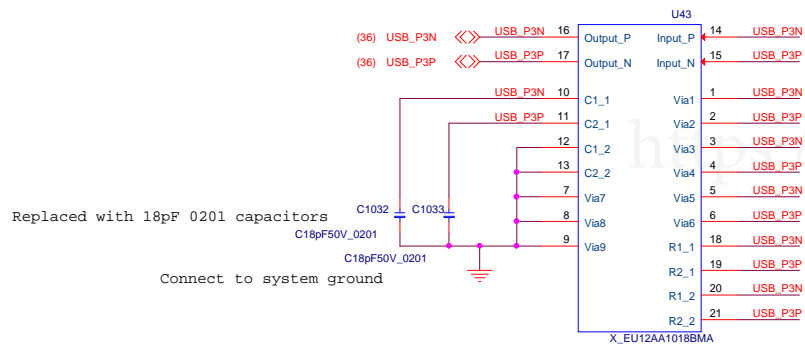
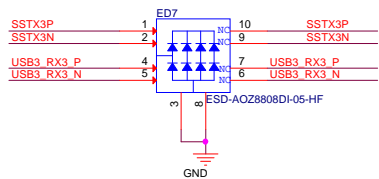
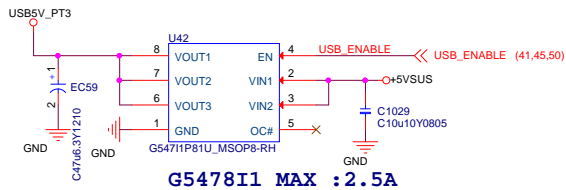


LAN (E2500)

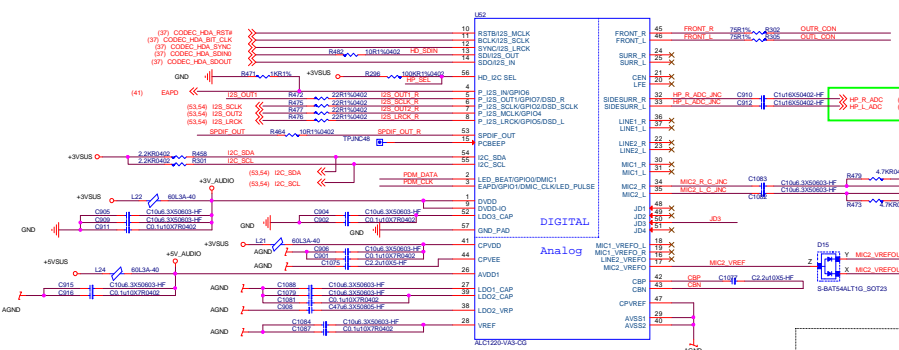




USB 3.0 CNT 3

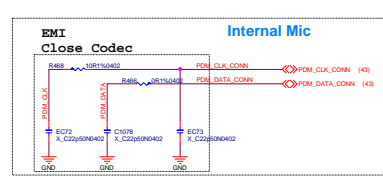
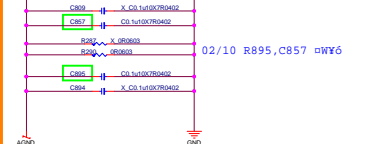
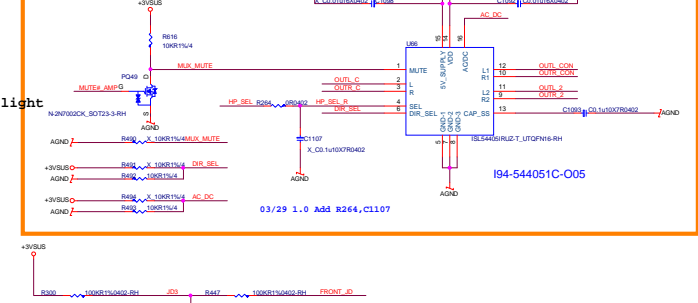


USB3.0	N53-09M0681-AF2
USB3.0_LED	N53-13M0031-L06

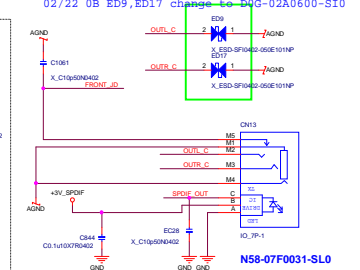
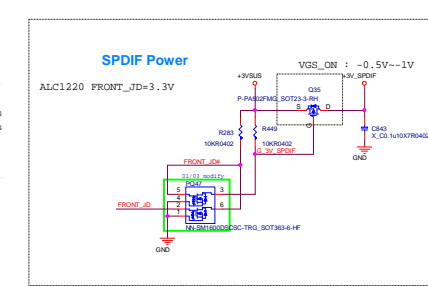
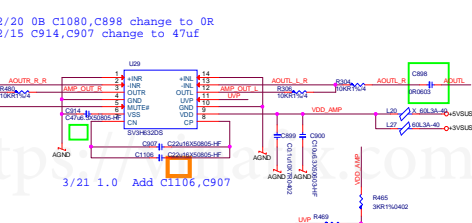
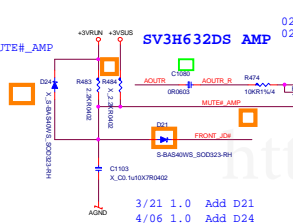
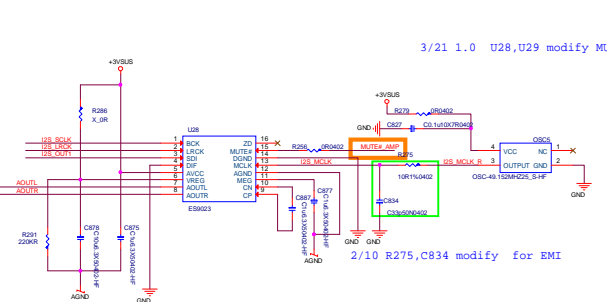
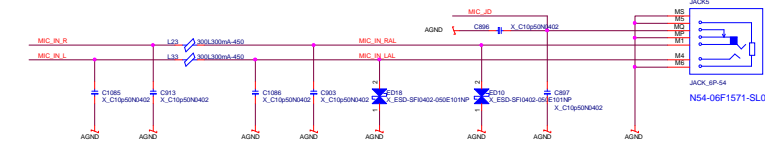


key board light

MIC



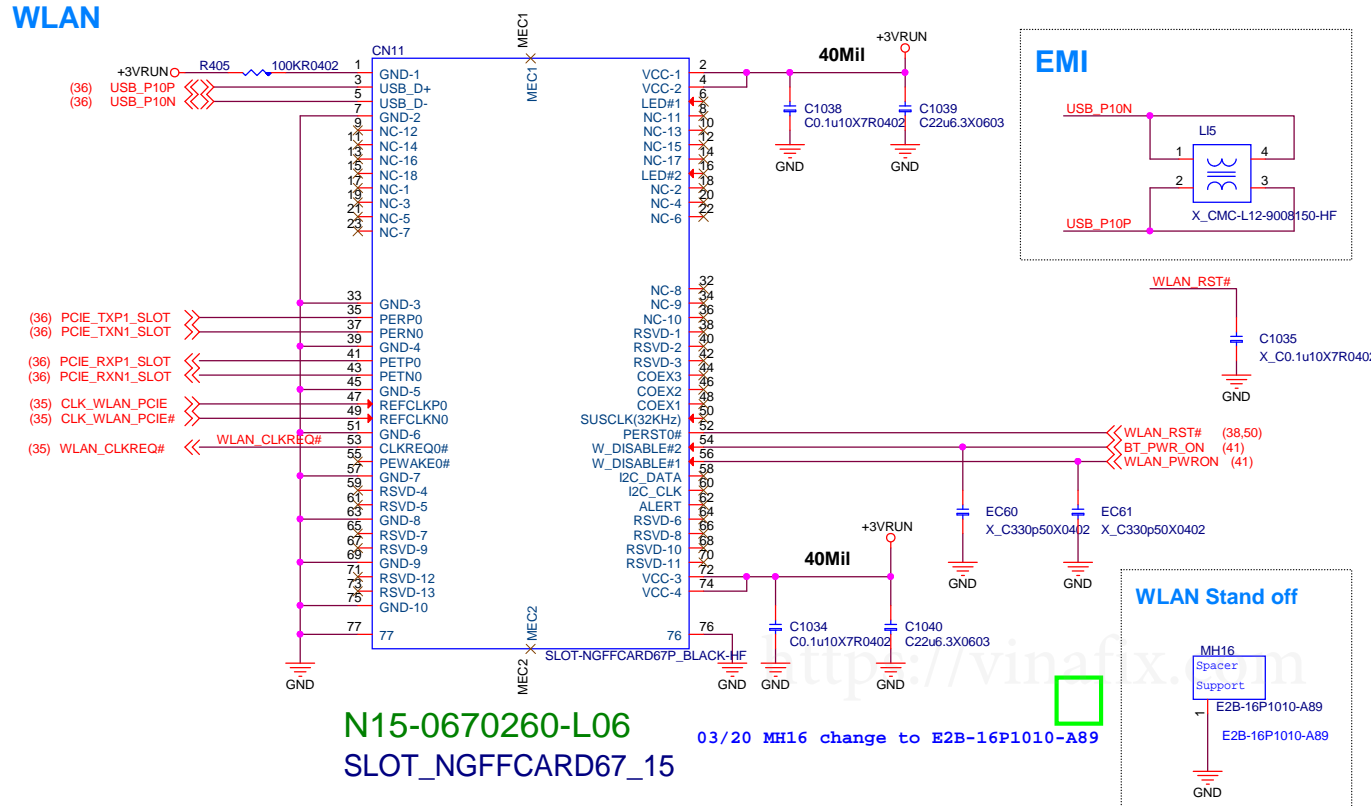
MIC IN



1. 0V10V	0. 0V	0. 0V
2. 0V10V	0. 0V	0. 0V

WLAN /Touch Pad

WLAN



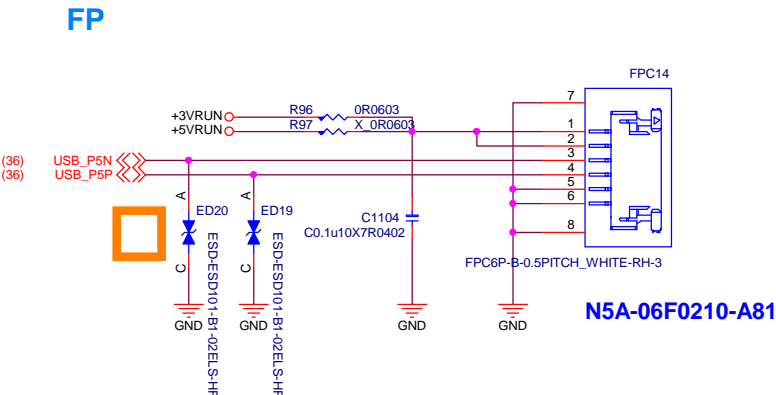
N15-0670260-L06

03/20 MH16 change to E2B-16P1010-A89

SLOT_NGFFCARD67_15

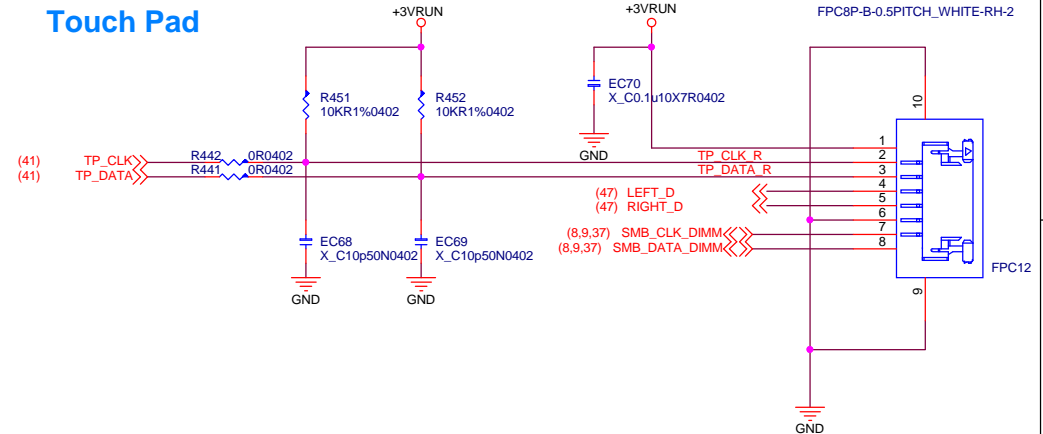
03/21 1.0 Add FPC14

FP



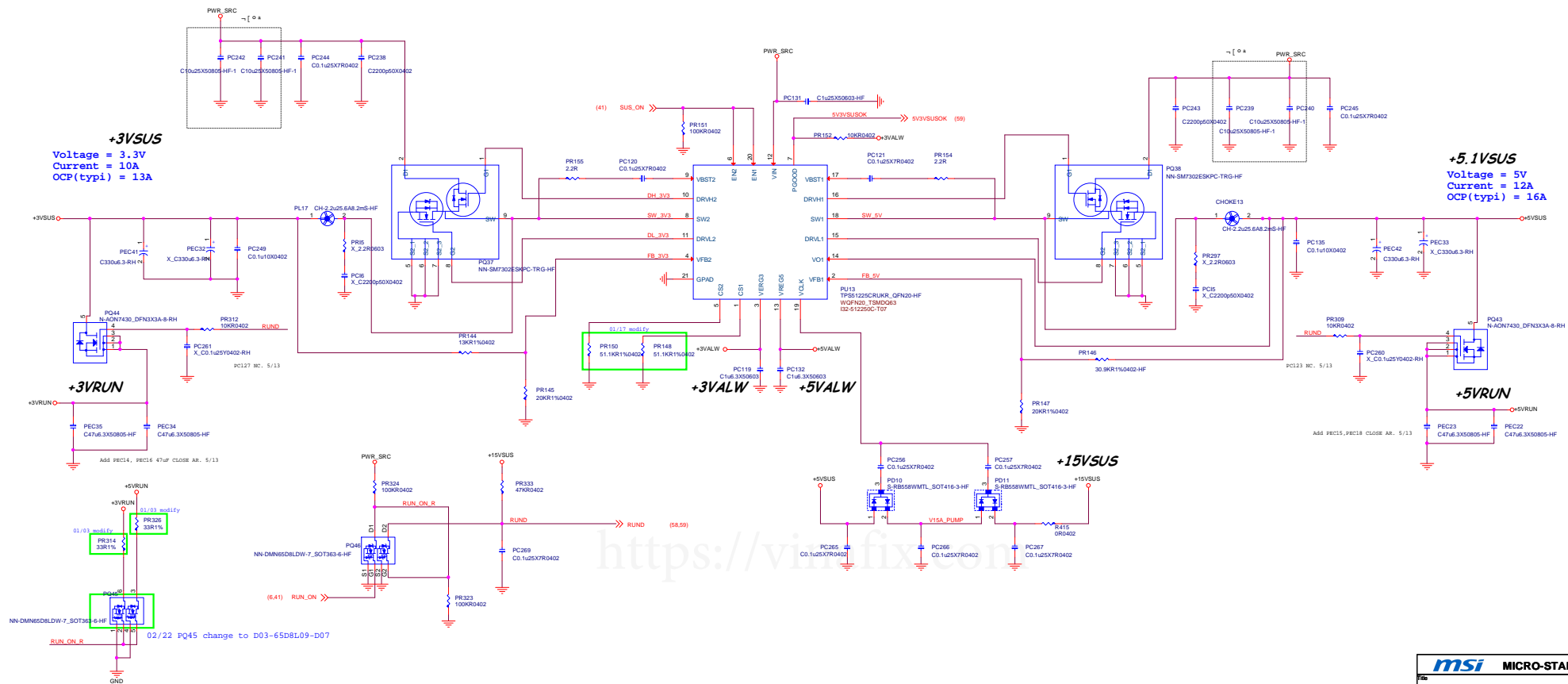
04/06 1.0 Add ED19,ED20

Touch Pad

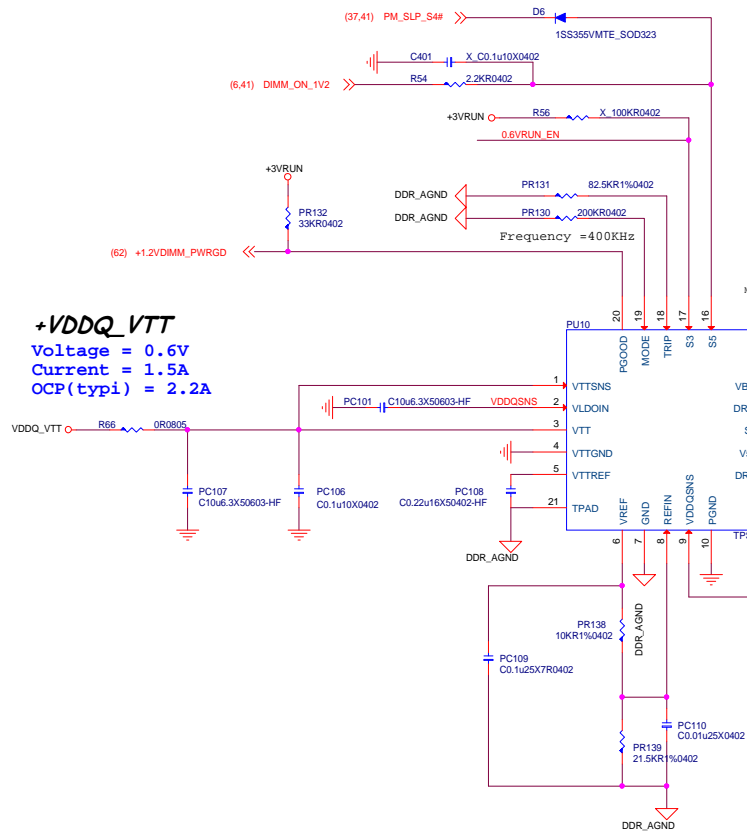


msi MICRO-STAR INT'L CO.,LTD.

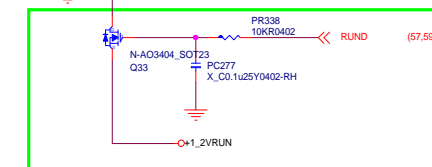
Title	WLAN /ClickPad		
Size	Document Number	Rev	
Custom	MS-16P11	0A	
Date:	Wednesday, May 03, 2017	Sheet	55 of 82



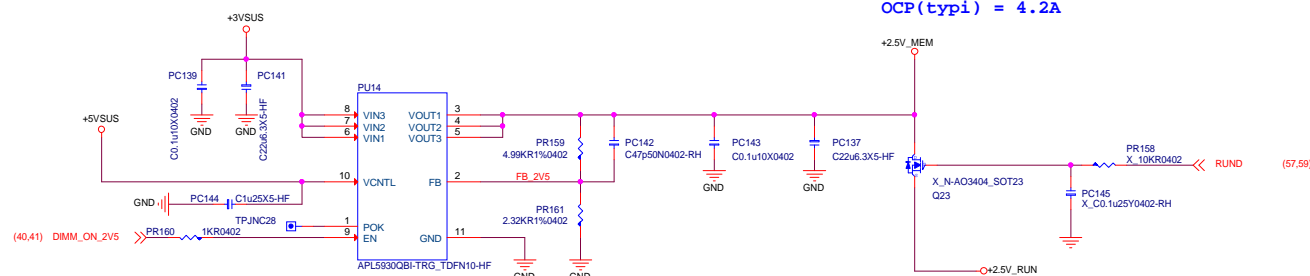
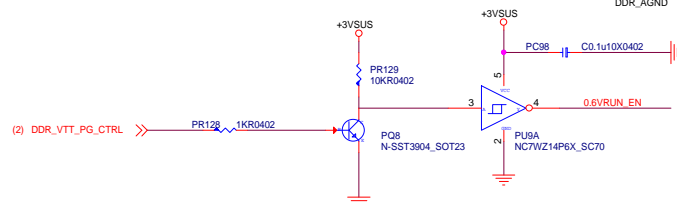
+VDDQ_VTT
 Voltage = 0.6V
 Current = 1.5A
 OCP(typi) = 2.2A



+1.2VDIMM
 Voltage = 1.2V
 Current = 9A
 OCP(typi) = 12A



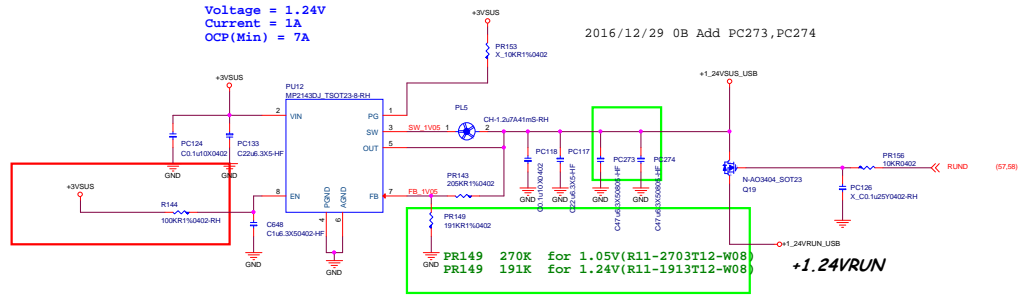
+2.5V_MEM
 Voltage = 2.5V
 Current = 0.4A
 OCP(typi) = 4.2A



+1.24VSUS

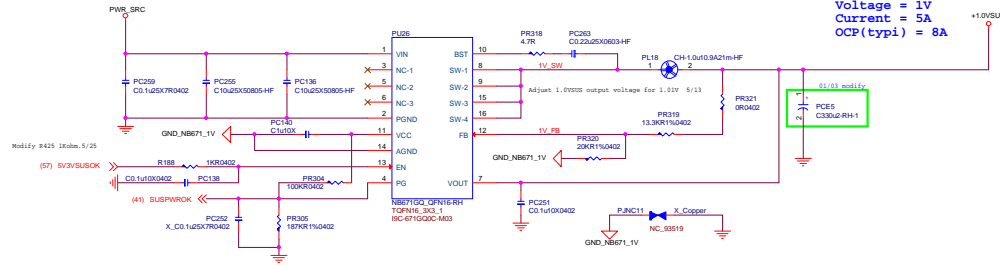
Voltage = 1.24V
Current = 1A
OCP(Min) = 7A

2016/12/29 0B Add PC273,PC274



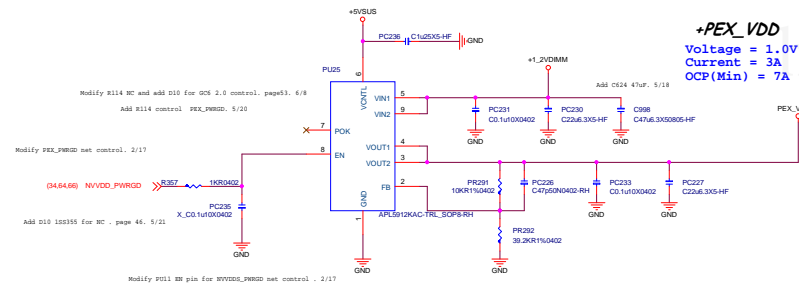
+1.01VSUS

Voltage = 1V
Current = 5A
OCP(typi) = 8A



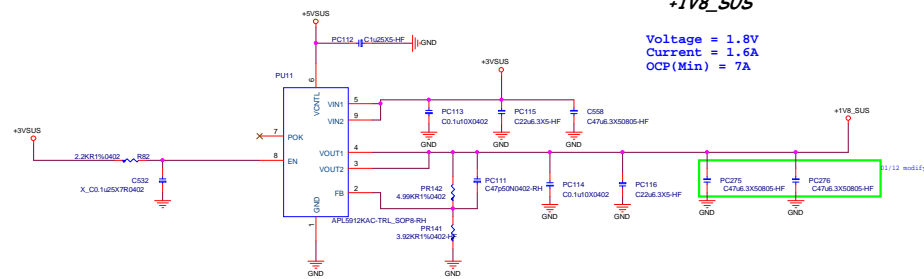
+PEX_VDD

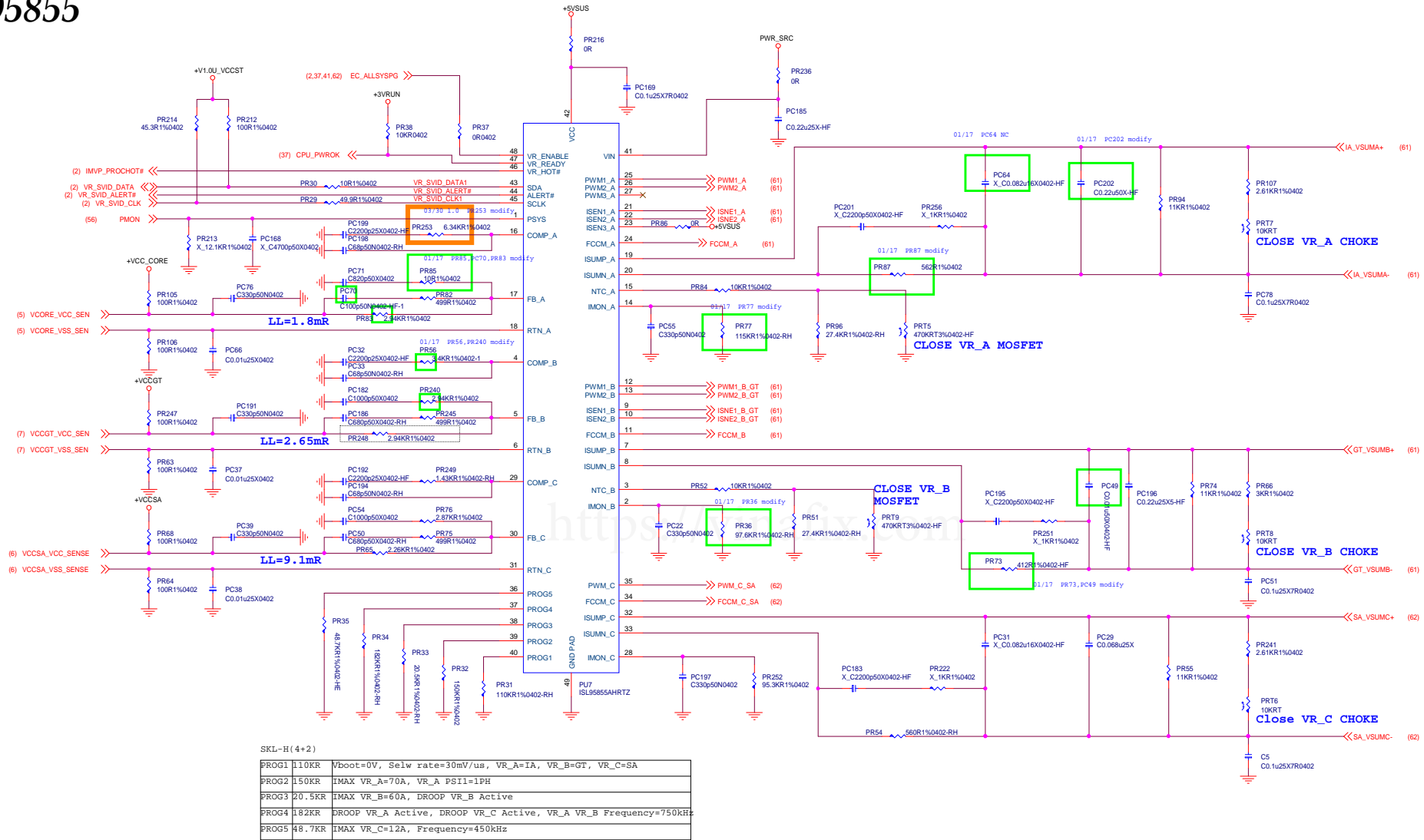
Voltage = 1.0V
Current = 3A
OCP(Min) = 7A



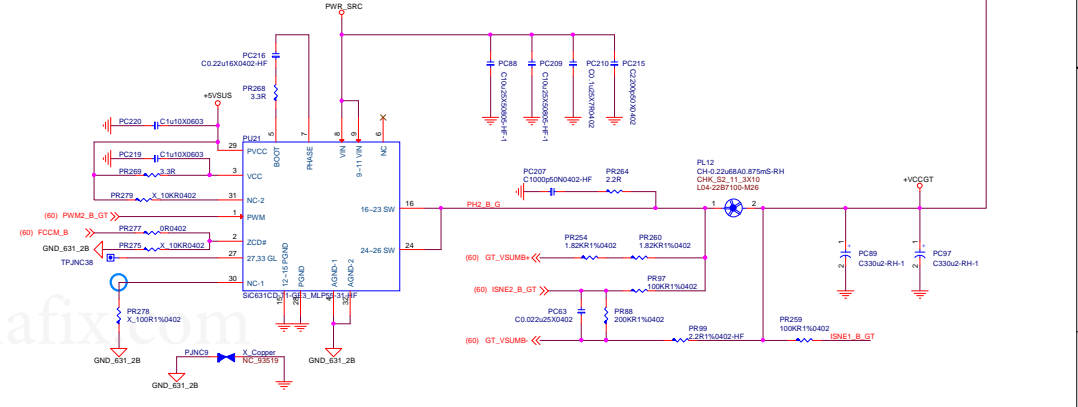
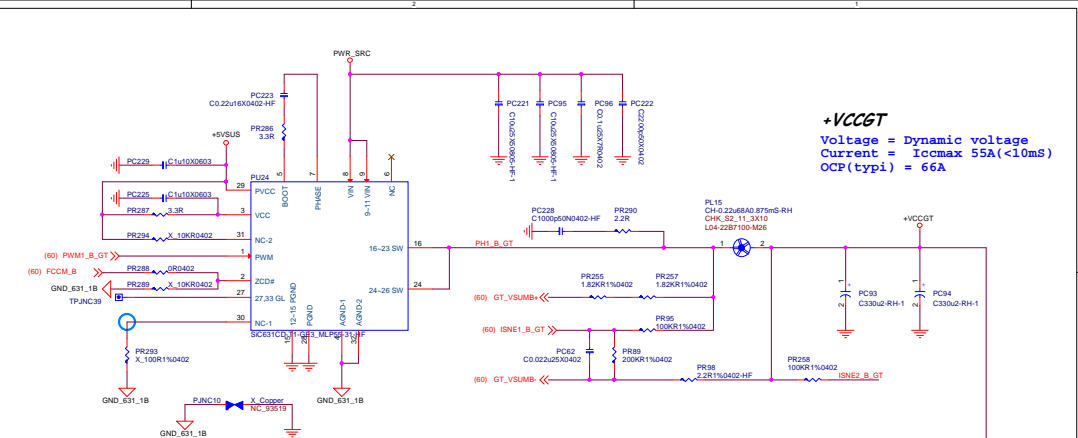
+1V8_SUS

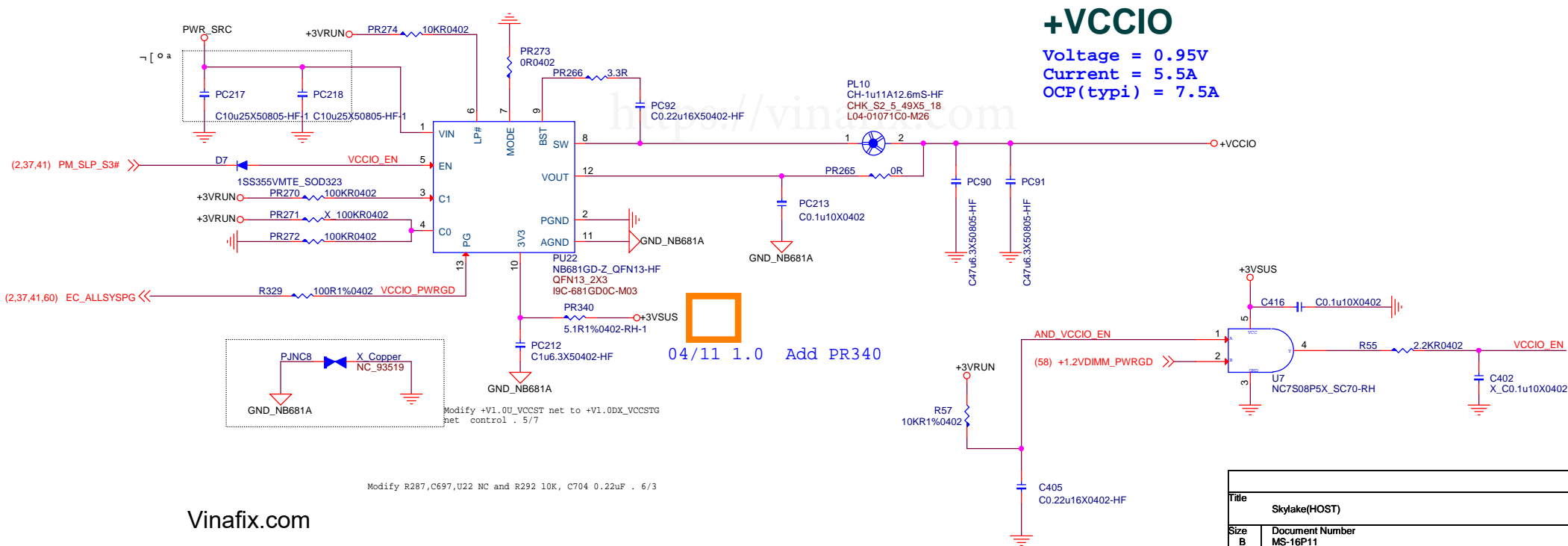
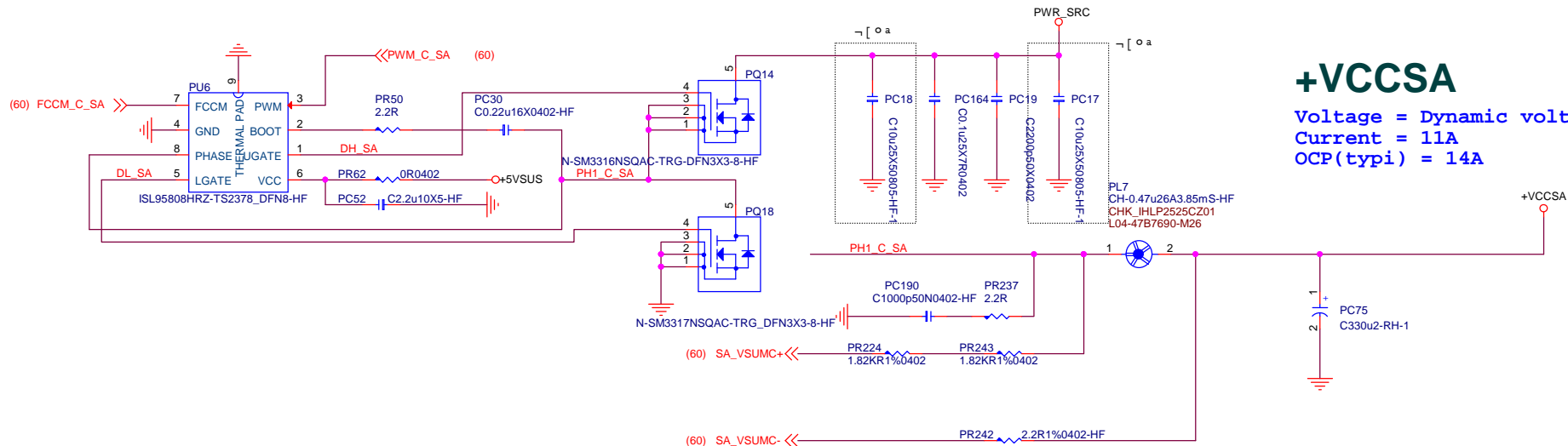
Voltage = 1.8V
Current = 1.6A
OCP(Min) = 7A



Skylake H-line 42 45W
ISL95855

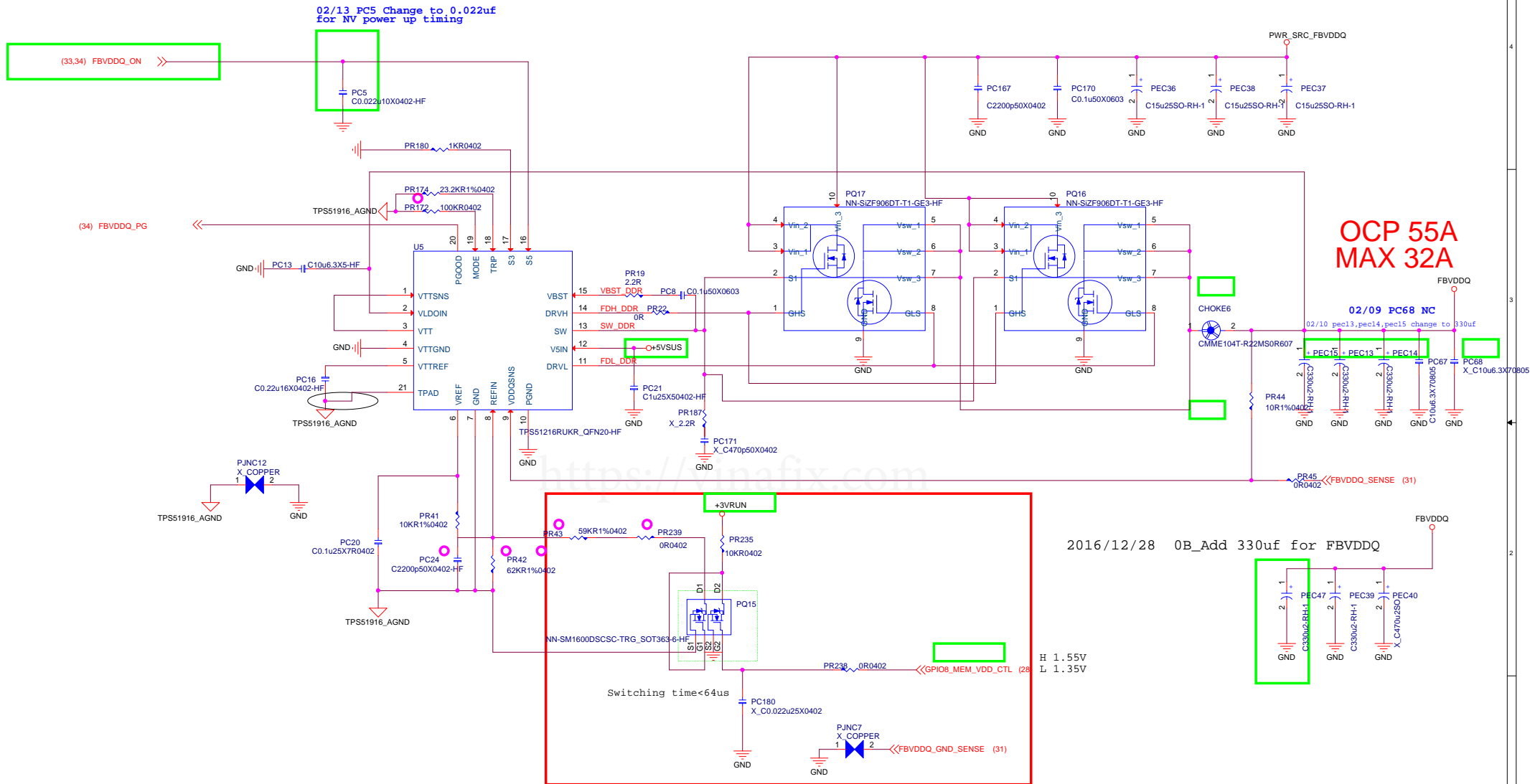
SKL-H (4+2)	
PROG1 110KR	Vboot=0V, Selw rate=30mV/us, VR_A=IA, VR_B=GT, VR_C=SA
PROG2 150KR	IMAX VR_A=70A, VR_A PSII=1PH
PROG3 20.5KR	IMAX VR_B=60A, DROOP VR_B_Active
PROG4 182KR	DROOP VR_A_Active, DROOP VR_C_Active, VR_A VR_B Frequency=750KHz
PROG5 48.7KR	IMAX VR_C=12A, Frequency=450KHz






Vinafix.com

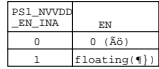
Title		
Skylake(HOST)		
Size	Document Number	Rev
B	MS-16P11	0A
Date:	Wednesday, May 03, 2017	Sheet 62 of 82



 MICRO-STAR INT'L CO.,LTD.	
Title	FBVDDQ
Size	Document Number MS-16P11
Date:	Sheet 63 of 82
	Rev 0A

EDP-Peak 204A
EDP-Con 80A

VBoot:0.8V
Vmin:0.3V / Vmax:1.3V

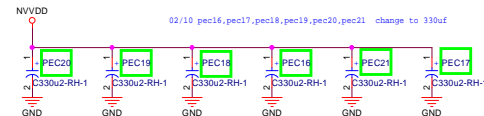
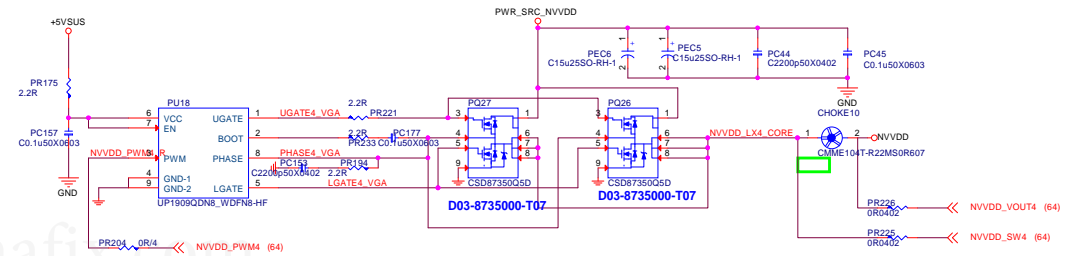
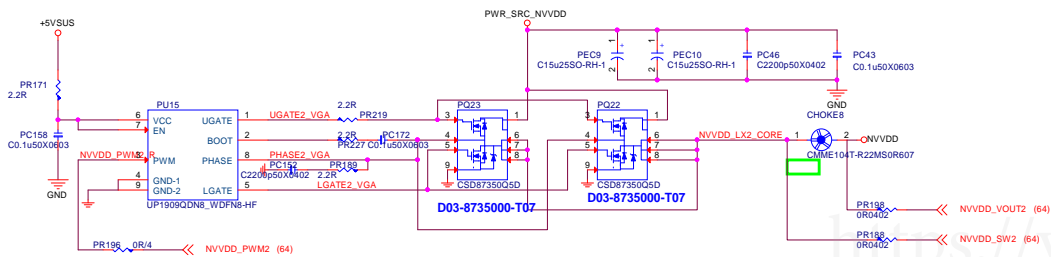
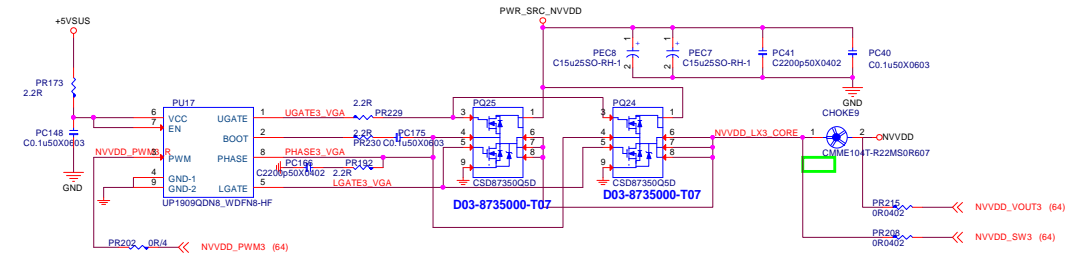
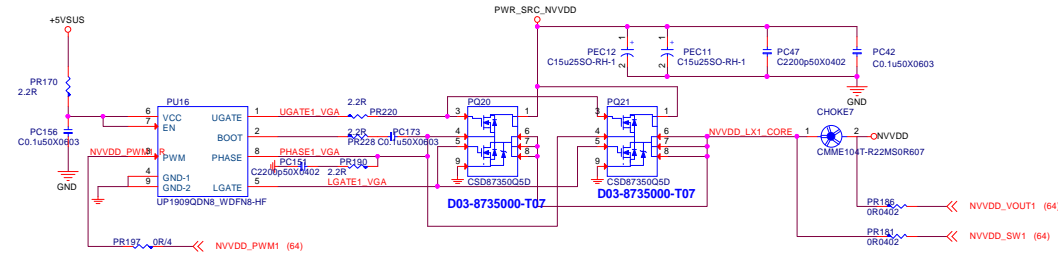


	PR885	PR897	PR92	PR104	PR1208	PC76
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	1.5nF

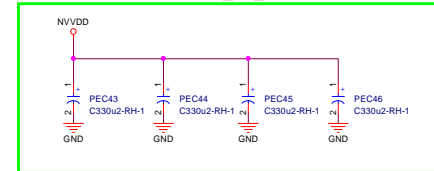
DGPU POWER

EDP-Peak 300A

EDP-Con 115A



2016/12/28 MS-16P11_0B_Add 330uf for NVDD



File	<Title>	Rev	0A
Size	Document Number	MS-16P11	0A
Customer	MS-16P11	0A	0A
Date	Wednesday, May 03, 2017	Sheet	65 of 82

EDP-Peak 74A
EDP-Con 28A

VBoot:0.8V
Vmin:0.5V / Vmax:1.25V

[Fugun] PR41 0ohm to 2.2ohm

2016/01/18 NV suggest un-stuff PR27

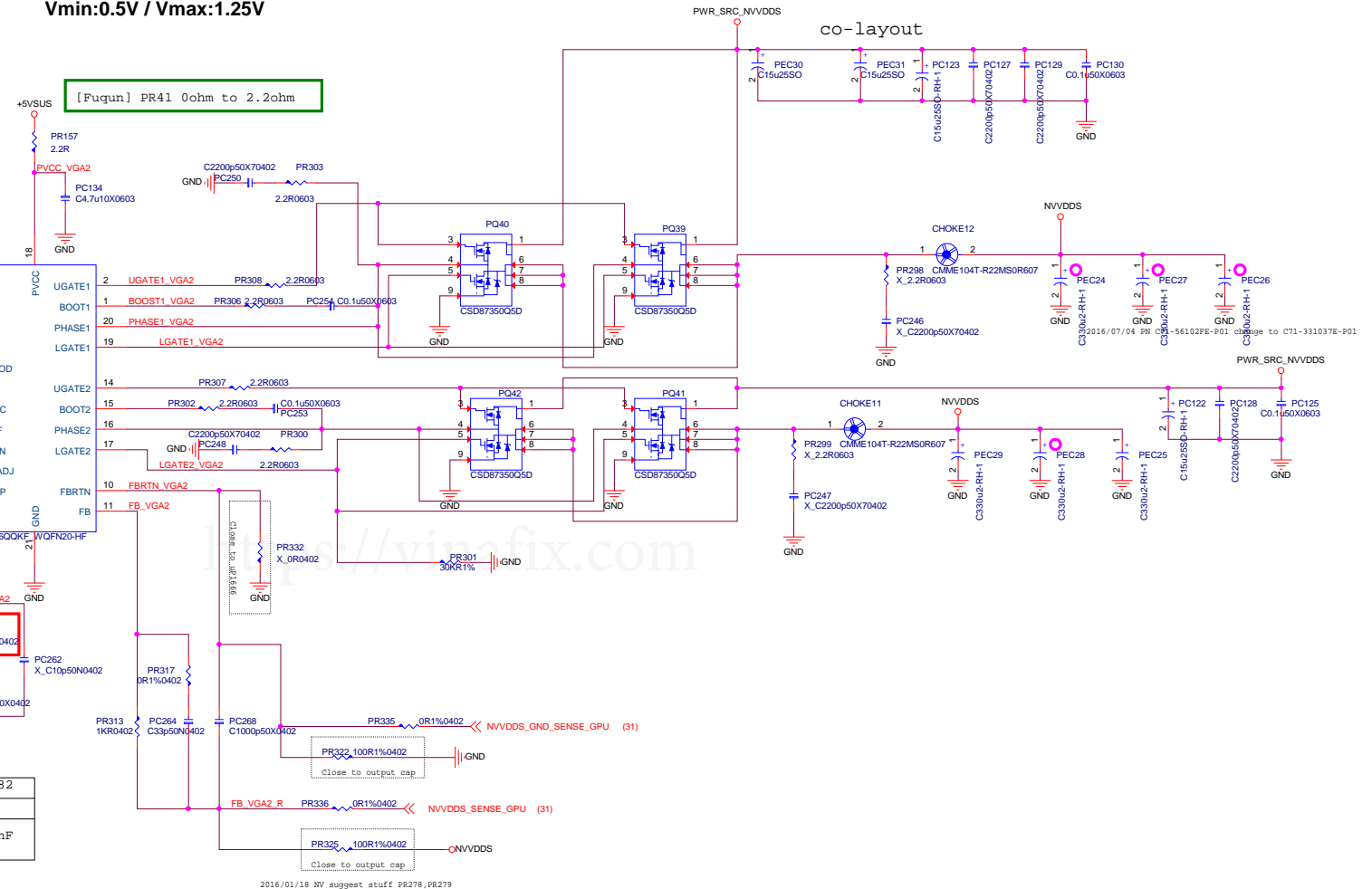
```
(28,64) GPIO6_NVVDD_PSI# >>
```

```
(28) GPIO3_NVVDDS_PWM_GPU >>
```

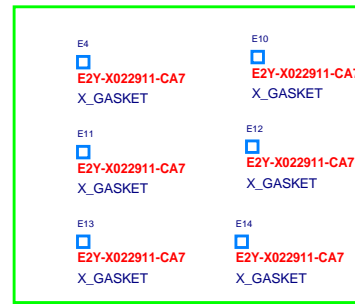
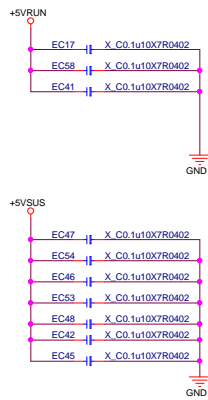
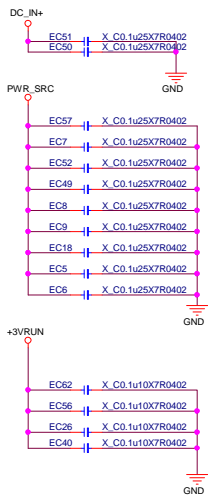
(34) NVVDDS_PWRGD <

[Fugun] Mount PR18
NC PR20

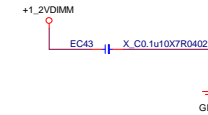
	PR311	PR309	PR308	PR307	PR310	PC282
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	4.7nF



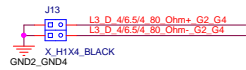
2016/01/18 NV suggest stuff PR278,PR279



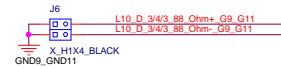
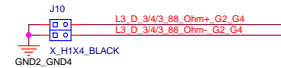
Add E4, E5, E6, E7, E8, E9 for EMI.5/22



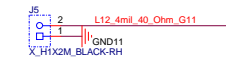
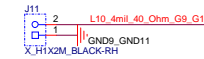
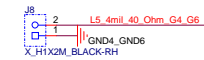
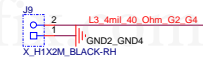
80 OHM / CLK/WCK



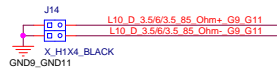
88 OHM /Alpine Ridge/DDR4 CLK



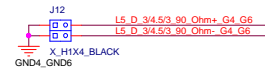
40 OHM / DDR4 CTRL



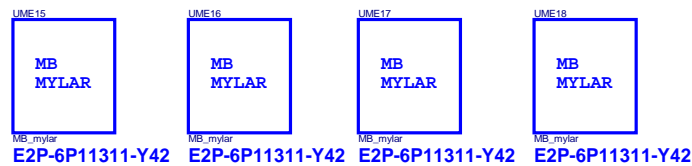
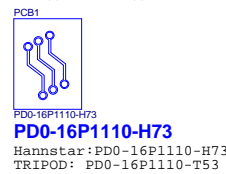
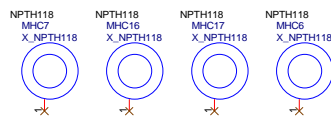
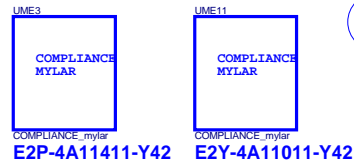
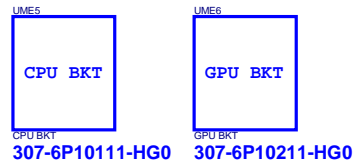
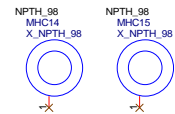
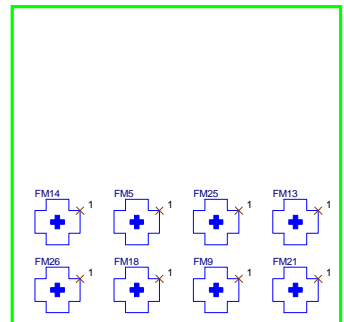
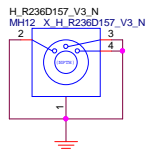
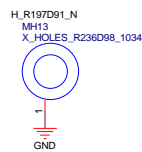
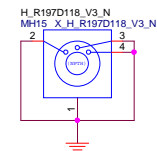
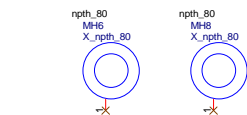
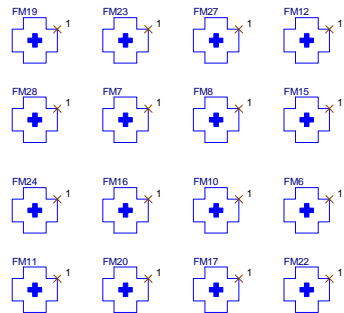
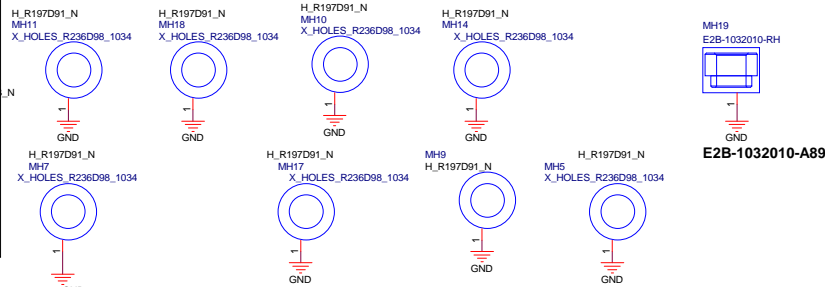
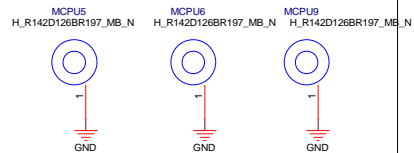
85 OHM /SATA /PCH PCIE/ EDP USB /HDMI/DP/DMI/CLK/PEG



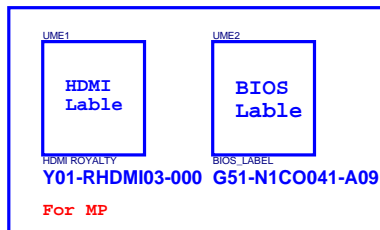
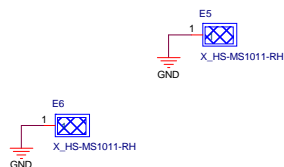
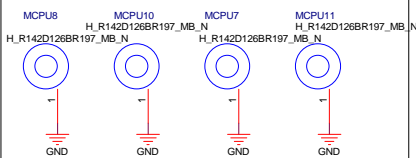
90 AR type-C



CPU Holes



DGPU Holes

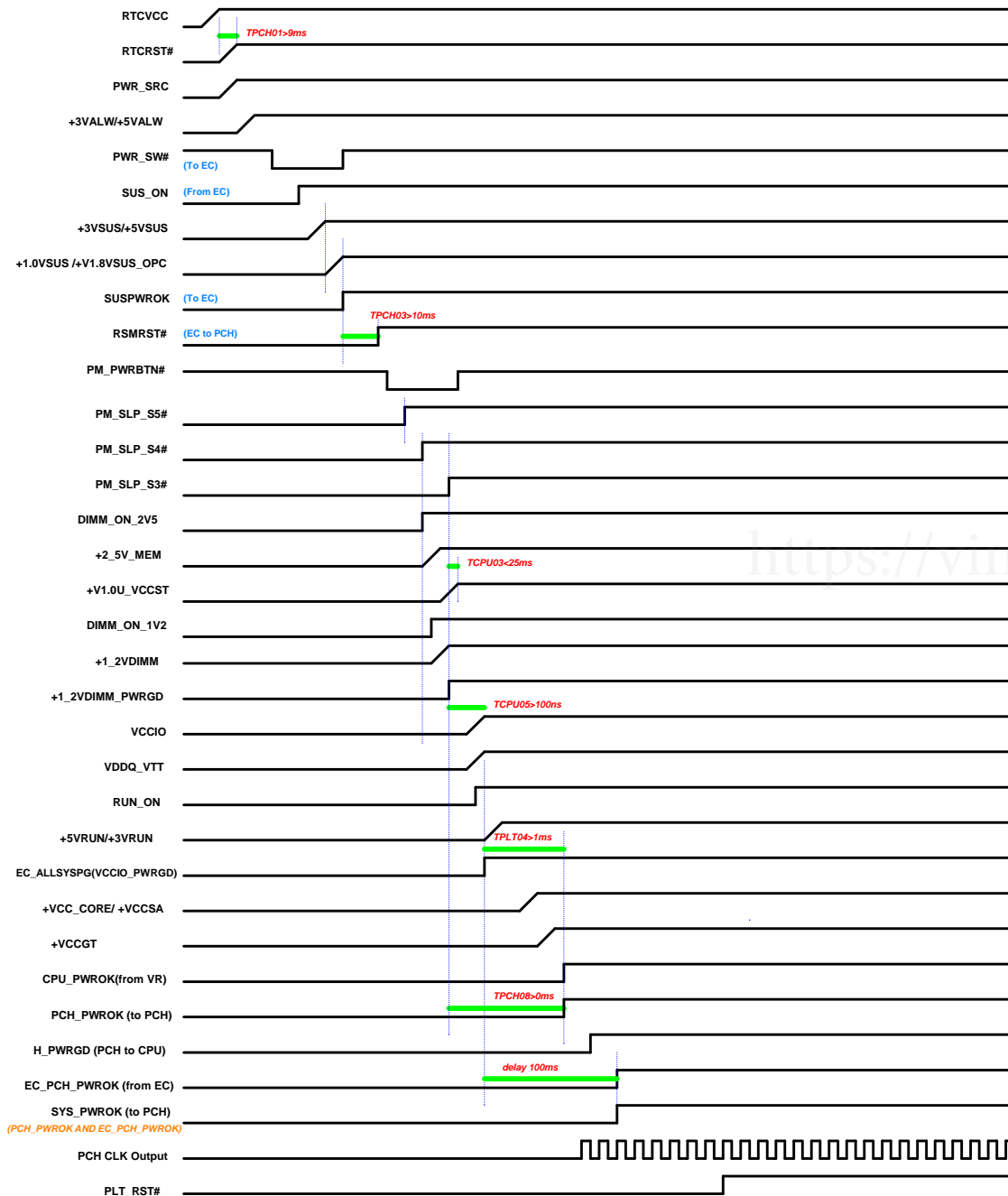


MS-16P1 Power Delivery Chart

<https://vinafix.com>

Power on Sequence

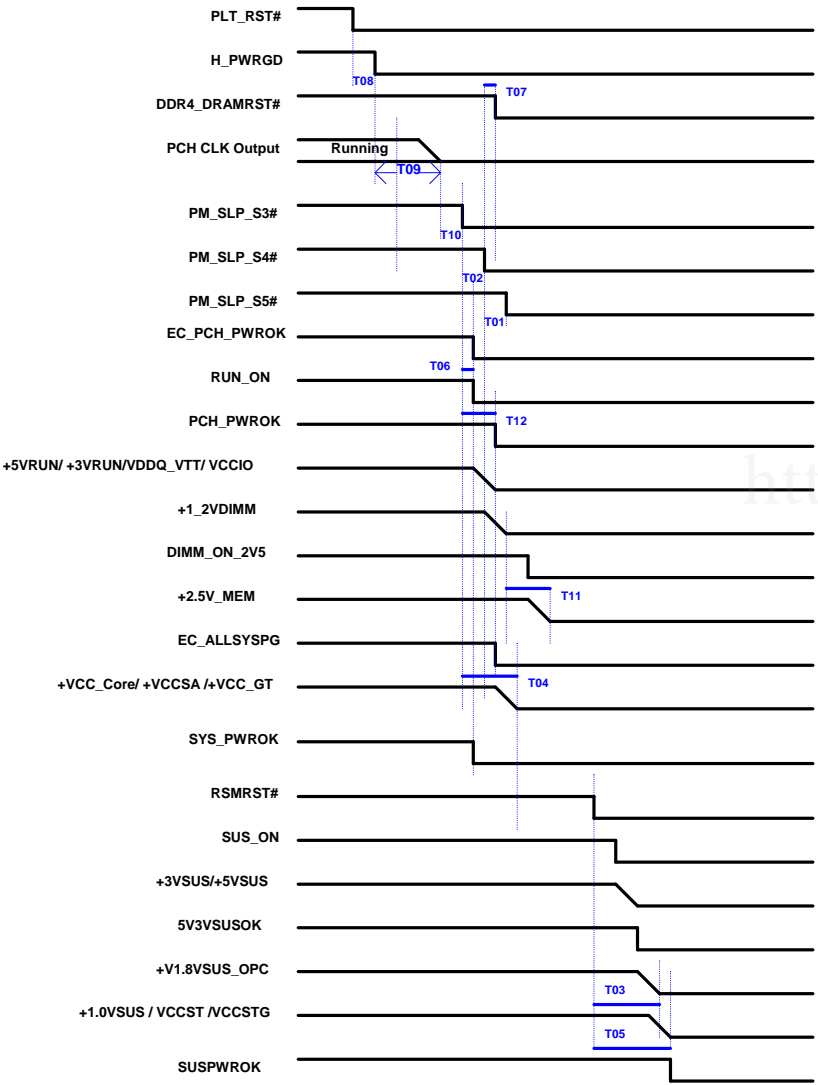
G3 -> S0



Vinafix.com

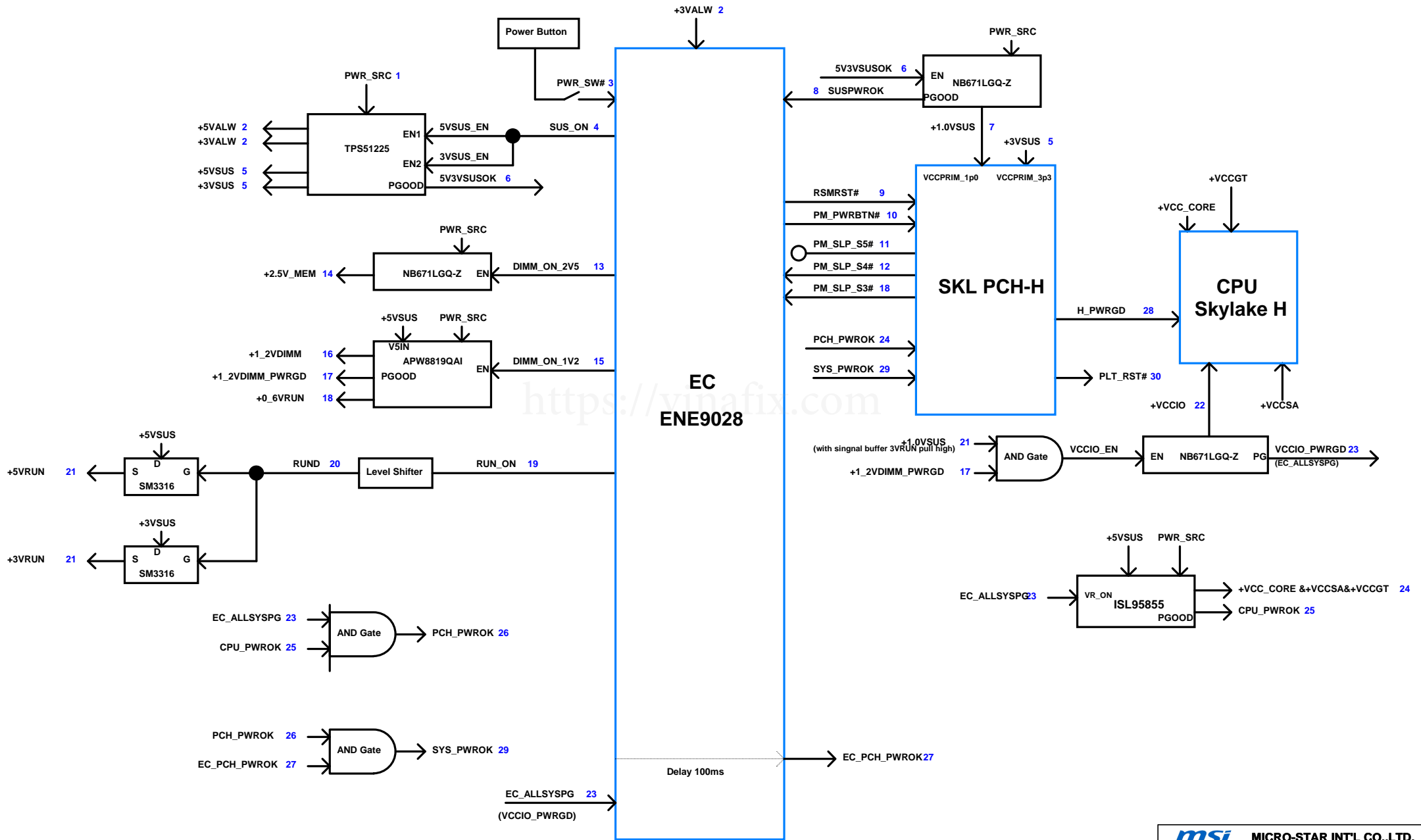
Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

MS-16P1 Power on Block Diagram



0B:

2017/01/03

- 1. PC85 P/N change to C71-33102AE-P01 on page59.
- 2. PQ47, PQ11, P09, PQ36, PQ10, PQ45 P/N change to D03-138DW19-D07 on page33, 52, 57..
- 3. R88, PR135, R64, PR140, R70, PR314, PR326 modify resistor value on page33, 57

2017/01/12

- 1. C175, C176, C177, C180, C181, C260, C285 P/N change to C11-4767314-M09 on page25.
- 2. Add PC275, PC276 on page 59
- 3. C370, C373 Change to 47uf/0805 on page10, 27
- 4. Add +1.2VDRN page58
- 5. Add HDMI Retimer page46

2017/01/16

- 1. CN12 change to N53-09M0681-AF2

2017/01/17

- 1. PR150, PR148 \$I51.1K R11-5112T12-Y01
- 2. PR2950W6
- 3. PC237 \$12.2nF C11-2222022-Y01
- 4. PR253 \$13K R11-0302T12-Y01
- 5. PR85 \$1 10K R11-0100T12-Y01
- 6. PC70 \$1 100p C11-1011042-M09
- 7. PR83 \$1 2.94K R11-2941T12-Y01
- 8. PR56 \$1 3.4K R11-0342T12-Y01
- 9. PR240 \$1 2.94K R11-2941T12-Y01
- 10. PC64 \$1 NDC0W6
- 11. PC202 \$1 0.22uF C11-2242813-Y01
- 12. PR87 \$1 562K R11-5620T12-Y01
- 13. PR77 \$1115K R11-1157T12-Y01
- 14. PR36 \$1 97.6K R11-9762T12-Y01
- 15. PR73 \$1412R R11-4120T12-Y01
- 16. PC49 \$10.01uF C11-1032822-Y01

- 17. CN14, CN15 change to N15-0670320-CK3

2017/01/20

- 1. CN12 change to N53-13M0031-L06
- 2. Add Q40 for USB3.0LED

2017/01/23

- 1. PR108 change to 169K
- 2. Modify U64 pin17, 18 Pin defin

2017/01/25

- 1. Modify CN12 pin define

2017/02/06

- 1. R481 NC, R483 0W6
- 2. Add LED7 for17"

2017/02/08

- 1. R86, R93 change to 0603

2017/02/09

- 1. Add CN17, add A_LED_SCL, A_LED_SDA net
- 2. U28 modify HP_SKL

2017/02/10

- 1. Add SW5, SW7 for 17"
- 2. Delete E7
- 3. C438, C340, C944, PEC13, PEC14, PEC15, PEC16, PEC17, PEC18, PEC19, PEC20, PEC21 change to 330uf
- 4. R895, C857 0W6
- 5. R275, C834 modify for EMI
- 6. Add R614, R615

2017/02/13

- 1. C856, C797, C777, C795 change to C11-1062617-S02
- 2. PC5 Change to 0.022uf

2017/02/14

- 1. Add Q43, Q45, Q46 for audio impedance sense

2017/02/17

- 1. R242, R236, R235, R246, R234, R233 change to 0R
- 2. R165 NC, R170 0W6

2017/02/22

- 1. R09, RD17 change to D00-02A0600-S10
- 2. Q8, Q12, Q43, PQ45 change to D03-65D8L09-D07

2017/03/02

- 1. C735 change to C11-1052613-S02

2017/03/20

- 1. M816 change to E28-16P1010-A89
- 2. FPC12 change to NSA-08P0130-H06
- 3. Add UME15, UME16, UME17, UME18
- 4. C856, C797, C777, C795 change to C11-2267618-M09

10:

2017/03/21

- 1. ADD U66
- 2. Add FPC14
- 3. modify SMP_SCL, SMP_SDA on Page.40.41
- 4. CN7 change to NSN-22F0401-AF2
- 5. Add R41-120S022-H29 A/u
- 6. U28, U29 modify MUTEX AMP
- 7. Add D21
- 8. U26, U27 modify MUTEX_SPK
- 9. ADD Nets EC.101
- 10. ADD C1106, C907

2017/03/24

- 1. Add CAMERA Power U54
- 2. Modify +3V_MICCAM on page.43
- 3. Add PU28 on Page.43
- 4. modify SCL3, SDA3 on Page.40.41

2017/03/26

- 1. Add R264, C1107
- 2. PR12, PR7 Change to 910K, 100K
- 3. Delete UME9

2017/03/30

- 1. Add R462, D22, D23, C1108, C1109
- 2. PR253 modify

2017/03/31

- 1. EL6 Mirror

2017/04/06

- 1. Add RD19, RD20
- 2. Add R619, R620, L28, L29, C1110
- 3. Add D24

2017/04/07

- 1. Add EL12.
- 2. Delete R15
- 3. R590 change to 6.2K
- 3. C795, C777, C856, C797 change to C71-150261G-S03
- 4. PC161, PC187, PC203 Change to C11-1067620-M09
- 5. CN12 \$160W

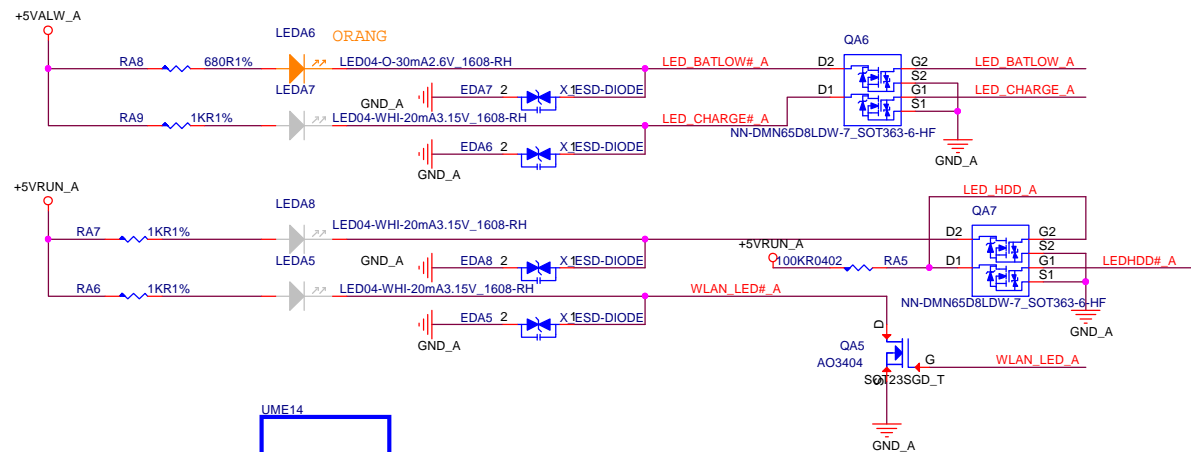
2017/04/10

- 1. Remove R622, R623

2017/04/11

- 1. Add PR340
- 2. Add R484

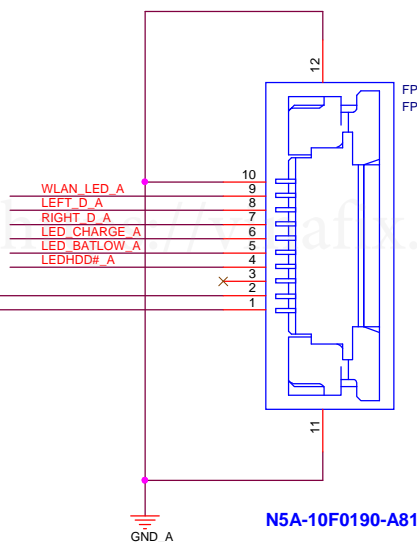
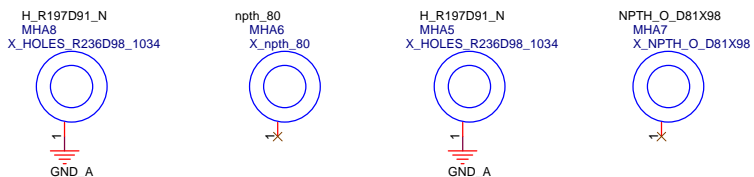
https://vinafix.com



UME14
 MB
 MYLAR
 POWER_ADHESIVE
 E2Y-6P11111-Y42

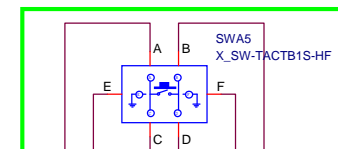
PCBA1
 PD0-16P1A10-H73
PD0-16P1A10-H73

Hannstar:PD0-16P1A10-H73
 TRIPOD: PD0-16P1A10-T53

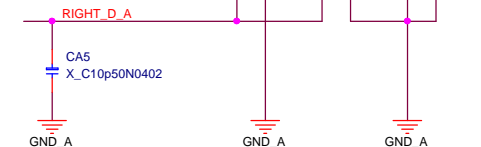


N5A-10F0190-A81

02/10 0B Add SWA5 for17"

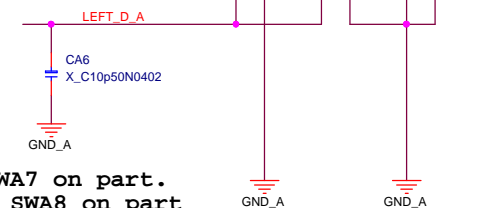
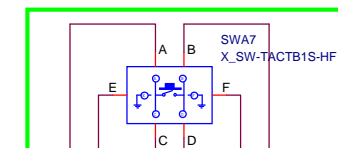


Touch Pad(A)



17" SWA5 on part.
 15.6" SWA6 on part

02/10 0B Add SWA7 for17"




17" SWA7 on part.
 15.6" SWA8 on part

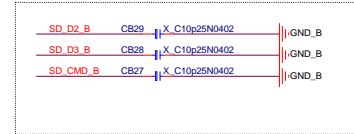
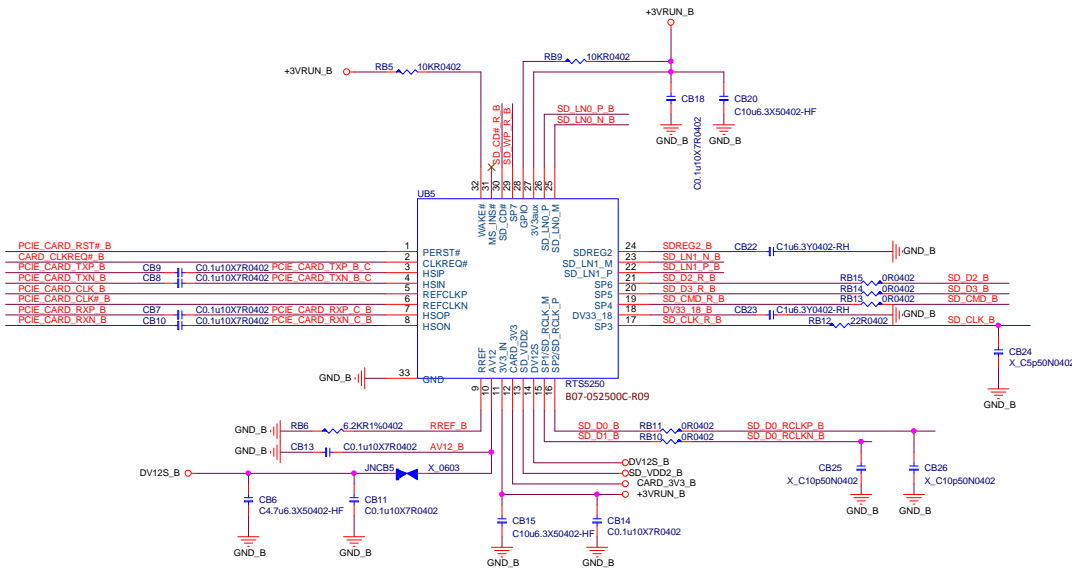
msi MICRO-STAR INT'L CO.,LTD.			
Title	[A] LED		
Size	Document Number	Rev	
Custom	MS-16P1A	0A	
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History

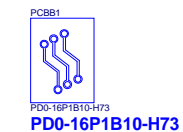
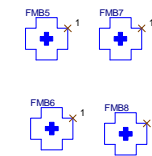
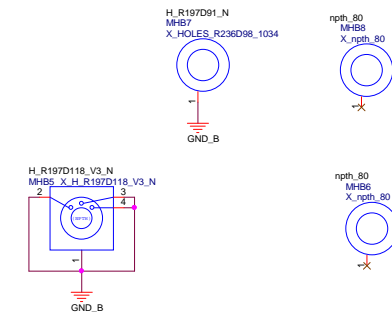
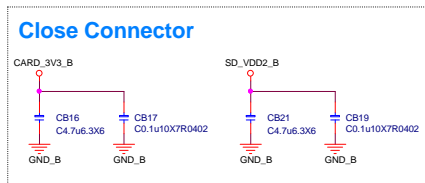
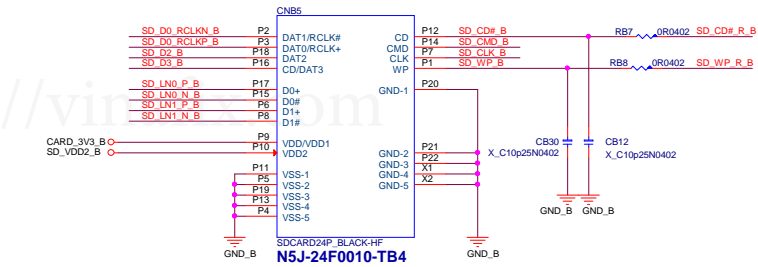
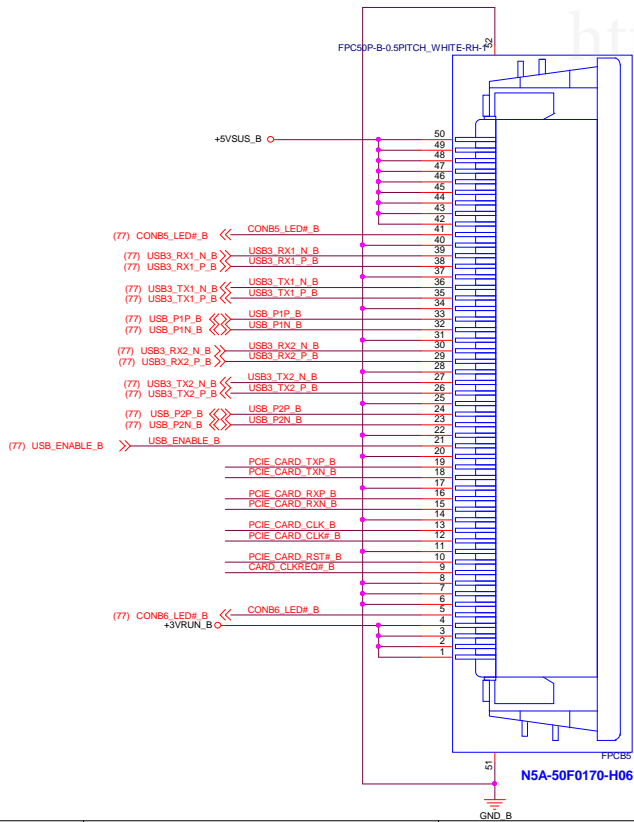
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CardReader (RTS5250)



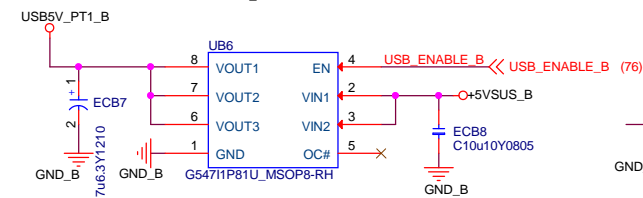
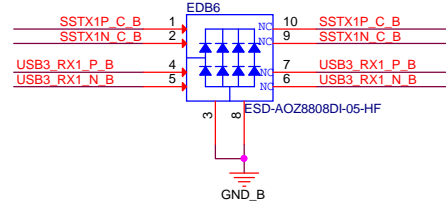
B to B



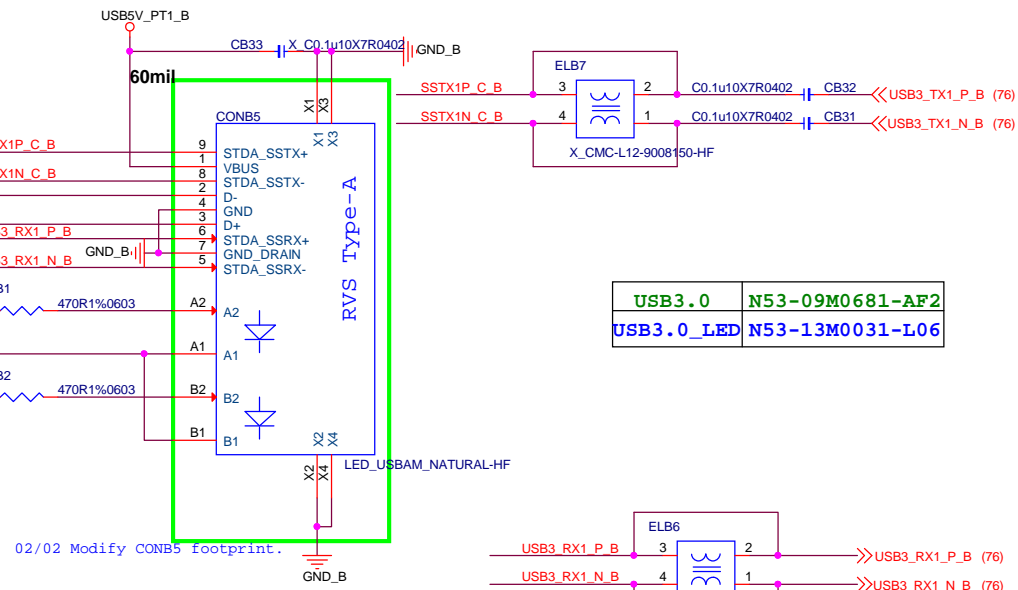
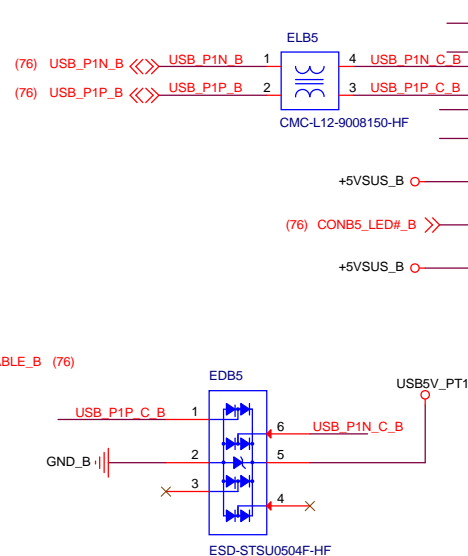
Hannstar:PD0-16P1B10-H73
TRIPOD: PD0-16P1B10-T53

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CardReader/BTB CONN			
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USB2.0/USB 3.0



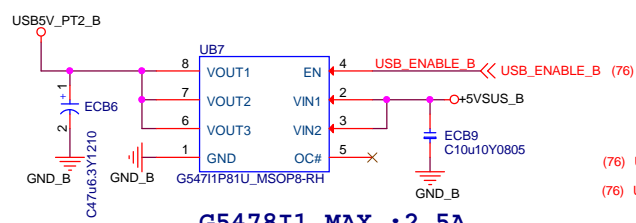
G5478I1 MAX :2.5A



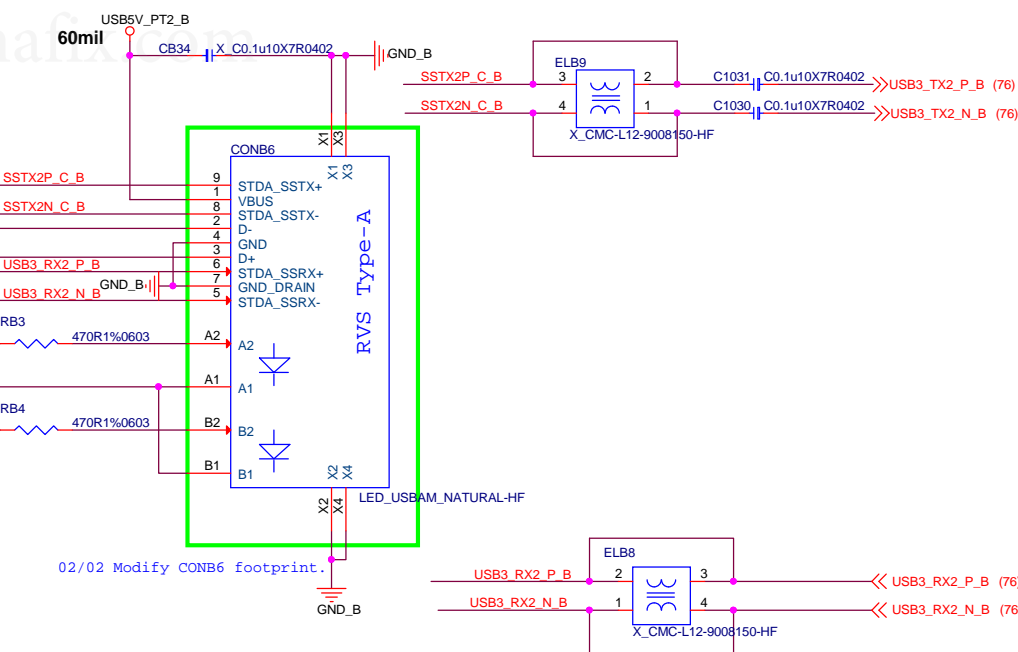
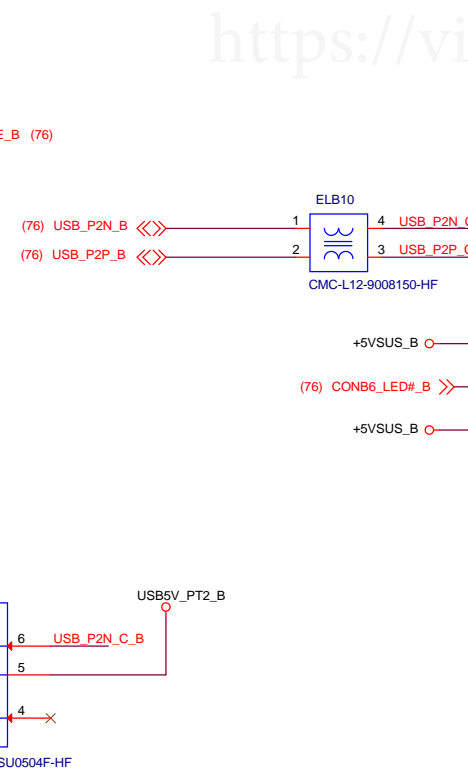
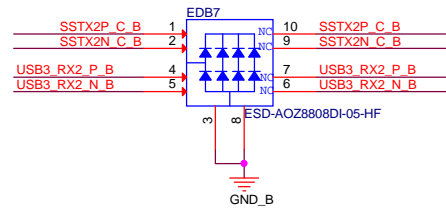
USB3.0	N53-09M0681-AF2
USB3.0_LED	N53-13M0031-L06

02/02 Modify CONB5 footprint.

USB 3.0 CNT 2



G5478I1 MAX :2.5A



02/02 Modify CONB6 footprint.

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2017/01/20

1. CONB5,CONB6 change to N53-13M0031-L06
2. Add QB1,QB2 for USB3.0LED

2017/01/25

1. Modify CONB5,CONB6 pin define

2017/02/08

1. RB1,RB2,RB3,RB4 change to 0603

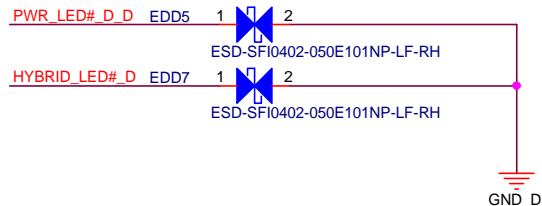
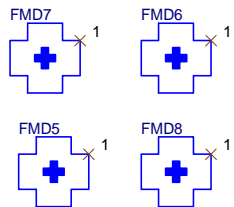
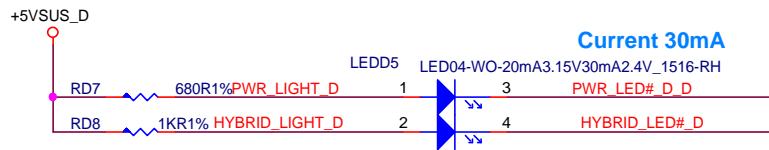
2017/04/07

1. CONB5,CONB6 500K

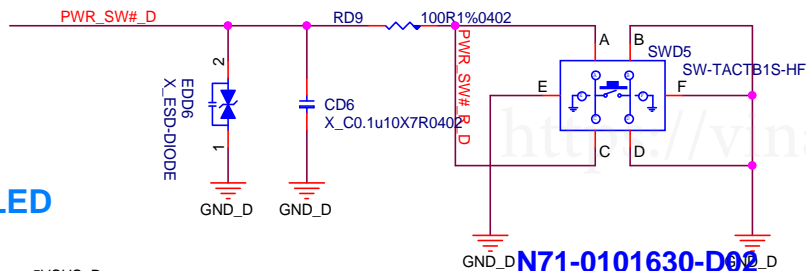
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<Title>			
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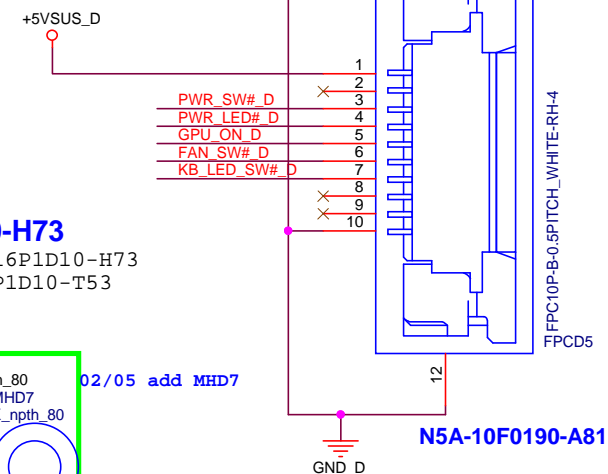
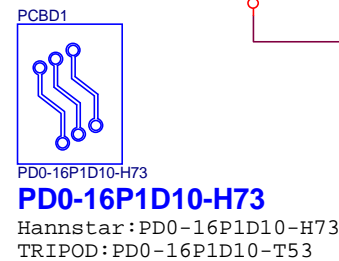
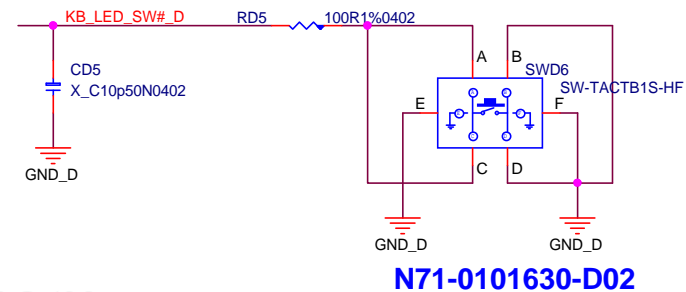
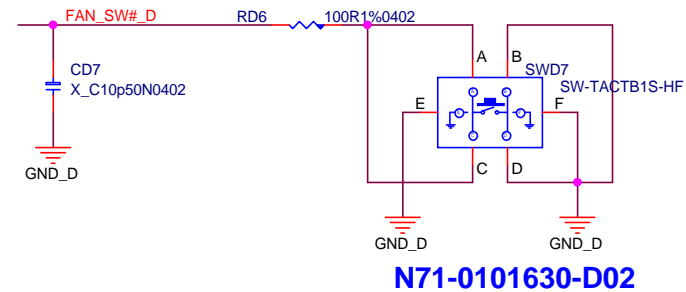
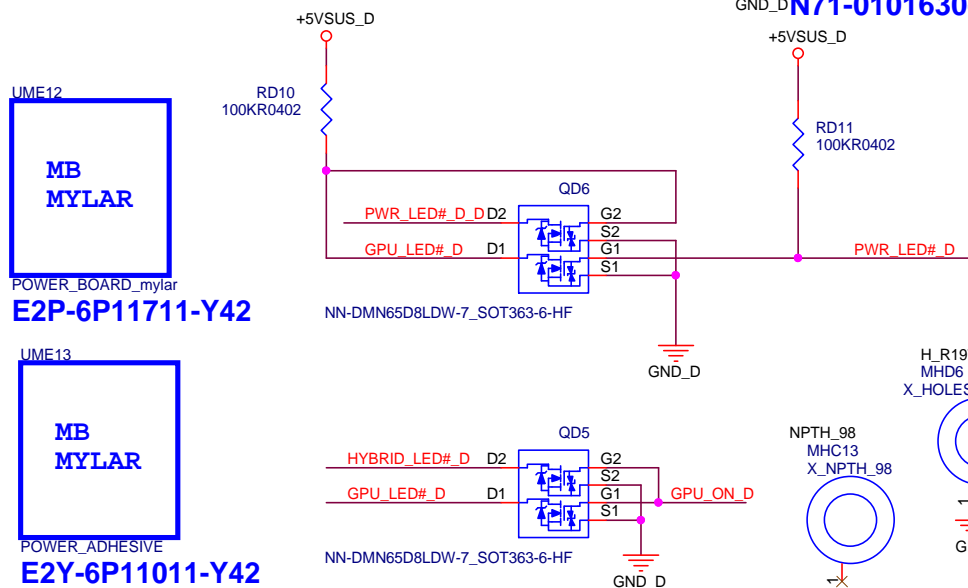
Power LED



Power Switch



Control PWR LED



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<Title>				
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2017/02/06

1. Add MHD7, delete MHC13

2017/02/09

1. Add MHC13

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TOP

16P11

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16P1C
for 15.6"
Power switch

16P1D
for 17"
Power switch

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